K.S.Rangasamy College of Technology

(Autonomous)

Curriculum & Syllabus

of

M.E. VLSI Design

(Batch admitted in 2025 – 2026)

R 2025

Accredited by NAAC with 'A++' Grade, Approved by AICTE,
Affiliated to Anna University, Chennai.

KSR Kalvi Nagar, Tiruchengode – 637 215.
Namakkal District, Tamil Nadu, India.

M.E. VLSI Design

Vision

To become recognized as a leader in Electronics and Communication Engineering education and research

Mission

- To craft professionals and technology leaders adherent to the professional ethical code in the areas of Electronics and communication Engineering
- To address the needs of the society while advancing boundaries of disciplinary and multidisciplinary research and cultivate universal moral values

PROGRAM EDUCATIONAL OBJECTIVES (PEOs)

PEO1: To develop a progressive career in research and industry with the ability to analyse, design and fabricate Integrated Circuits.

PEO2: To gain a firm grasp on growing areas of VLSI with acquired knowledge on concepts and use of appropriate tools

PEO3: To exhibit ethical practices and social behavior with an attitude of lifelong learning and strong communication skills

PROGRAMME OUTCOMES (POs)
Engineering Graduates will be able to:

PO1: An ability to independently carry out research /investigation and development work to solve practical problems
PO2: An ability to write and present a substantial technical report/document
PO3: Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program
PO4: An ability to identify appropriate EDA tool for design and analysis of Integrated Circuits
PO5: An ability to communicate effectively and solve societal problems with ethical principles
PO6: An ability to apply the knowledge of VLSI concepts in the design and development of Integrated Circuits

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

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MAPPING OF PROGRAMME EDUCATIONAL OBJECTIVES (PEOs) WITH PROGRAMME OUTCOMES (POs)

The M.E. VLSI Design Programme outcomes leading to the achievement of the objectives are summarized in the following Table.

Programme Educational Objectives	Programme Outcomes					
	PO1	PO2	PO3	PO4	PO5	PO6
PEO 1	3	3	3	3	3	2
PEO 2	3	3	3	3	3	3
PEO 3	2	2	2	2	2	3

Contributions: 1- low, 2- medium, 3- high

MAPPING: VLSI DESIGN (PG)

YEAR	SEM	COURSE CODE	COURSE NAME	PO1	PO2	PO3	PO4	PO5	PO6
I	I	70 PVL 101	Linear Algebra and Graph Theory	3	3			2	2.4
		70 PIS 001/ 70 PSE 001	Research Methodology and IPR	3	3	2	2	2	2
		70 PVL 102	Analog IC Design	3	3	3	2	2	3
		70 PVL 103	Digital IC Design	3	3	3	2	2	3
		70 PVL 104	Advanced Digital System Design	3	3	3	3	3	3
		70 PVL E1*	Professional Elective I						
		70 PAC 001	English for Research Paper Writing	3	3	2	3	3	3
		70 PVL 1P1	VLSI Laboratory I	3	3	3	2	2	3
		70 PVL 1P2	Analog IC Design Laboratory	3	3	3	3	2	3
	II	70 PVL 201	Solid State device Modelling and Simulation	3	3	3	3	2	3
		70 PVL 202	VLSI Design	3	3	2.6	2.4	2.6	2.6
		70 PVL 203	VLSI Testing	3	2.8	2.8	2.8	2.8	3
		70 PVL 204	ASIC Design	2.6	2	3	2.5	2.5	3
		70 PVL E2*	Professional Elective II						
		70 PVL E3*	Professional Elective III						
		70 PAC 002	Disaster Management	3	3	3		3	
		70 PVL 2P1	VLSI Laboratory II	3		3	3	3	3
		70 PVL 2P2	Term Paper and Seminar	3	2.75	3	2.4	2.75	3
II	III	70 PVL 301	Electronic Packaging	3	3	3	2	2	3
		70 PVL E4*	Professional Elective IV						
		70 PVL E5*	Professional Elective V						
		70 PVL 3P1	Project Work Phase I	3	3	3	3	3	3
	IV	70 PVL 4P1	Project Work Phase II	3	3	3	3	3	3

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PROFESSIONAL CORE (PC)

S. No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C	Prerequisite
1.	70 PVL 101	Linear Algebra and Graph Theory	PC	5	3	1	0	4	Discrete Mathematics
2.	70 PIS 001/ 70 PSE 001	Research Methodology and IPR	RM	3	3	0	0	3	Nil
3.	70 PVL 102	Analog IC Design	PC	3	3	0	0	3	Courses on Semiconductor Devices and Circuits and Linear IC Applications at UG Level
4.	70 PVL 103	Digital IC Design	PC	3	3	0	0	3	Digital logic design, VLSI Design
5.	70 PVL 104	Advanced Digital System Design	PC	5	3	1	0	4	Digital Logic Design
6.	70 PVL 1P1	VLSI Laboratory I	PC	4	0	0	4	2	Analog and Digital CMOS VLSI design
7.	70 PVL1P2	Analog IC Design Laboratory	PC	4	0	0	4	2	Courses on Semiconductor Devices and Circuits and Linear IC Applications at UG Level
8.	70 PVL 201	Solid State device Modelling and Simulation	PC	3	3	0	0	3	Semiconductor devices and circuits
9.	70 PVL 202	VLSI Design Automation	PC	3	3	0	0	3	Analog and Digital CMOS VLSI design
10.	70 PVL 203	VLSI Testing	PC	3	3	0	0	3	Analog and Digital CMOS VLSI design
11.	70 PVL 204	ASIC Design	PC	3	3	0	0	3	Digital Logic Design
12.	70 PVL 2P1	VLSI Laboratory II	PC	4	0	0	4	2	Basic Verilog HDL
13.	70 PVL 301	Electronic Packaging	PC	3	3	0	0	3	Electronic Circuits and Embedded Systems

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PROFESSIONAL ELECTIVE (PE)

SEMESTER I, PROFESSIONAL

ELECTIVE I

S.No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C	Prerequisite
1.	70 PVL E11	System Design with FPGA	PE	3	3	0	0	3	Digital system Design
2.	70 PVL E12	Advanced Computer Architecture	PE	3	3	0	0	3	Nil
3.	70 PVL E13	VLSI Digital Signal Processing	PE	3	3	0	0	3	Nil
4.	70 PVL E14	Machine Learning in VLSI Design	PE	3	3	0	0	3	Nil
5.	70 PVL E15	VLSI Technology	PE	3	3	0	0	3	Nil

SEMESTER II, PROFESSIONAL ELECTIVE II

S.No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C	Prerequisite
1.	70 PVL E21	Low Power VLSI Design	PE	3	3	0	0	3	Analog and Digital CMOS VLSI design
2.	70 PVL E22	Digital image Processing	PE	3	3	0	0	3	Image Processing
3.	70 PVL E23	IP Based VLSI Design	PE	3	3	0	0	3	Digital CMOS VLSI Design
4.	70 PVL E24	Genetic Algorithm for VLSI Design	PE	3	3	0	0	3	Nil
5.	70 PVL E25	Bio Signal Processing	PE	3	3	0	0	3	Digital Signal Processing

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SEMESTER II, PROFESSIONAL ELECTIVE III

S.No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C	Prerequisite
1.	70 PVL E31	VLSI for Wireless Communication	PE	3	3	0	0	3	Fundamentals of VLSI and Wireless Communication
2.	70 PVL E32	System on Chip	PE	3	3	0	0	3	Nil
3.	70 PVL E33	Design for Verification using UVM	PE	3	3	0	0	3	System Verilog
4.	70 PVL E34	FPGA Based Implementation of Signal Processing Systems	PE	3	3	0	0	3	Digital Logic Design and Digital Signal processing
5.	70 PVL E35	Wireless Sensor Networks	PE	3	3	0	0	3	Nil

SEMESTER III, PROFESSIONAL ELECTIVE IV

S.No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C	Prerequisite
1.	70 PVL E41	DSP Structures for VLSI	PE	3	3	0	0	3	Signal Processing
2.	70 PVL E42	Applied Medical Image Processing	PE	3	3	0	0	3	Nil
3.	70 PVL E43	Data Science and Engineering	PE	3	3	0	0	3	Nil
4.	70 PVL E44	Data Converters IC Design	PE	3	3	0	0	3	Nil
5.	70 PVL E45	Mixed Signal VLSI design	PE	3	3	0	0	3	Nil

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SEMESTER III, PROFESSIONAL ELECTIVE V

S.No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C	Prerequisite
1.	70 PVL E51	System Verilog	PE	5	3	0	2	4	Verilog HDL
2.	70 PVL E52	HDL for IC Design	PE	5	3	0	2	4	Digital System Design, Verilog HDL
3.	70 PVL E53	Deep Learning	PE	5	3	0	2	4	Machine Learning Techniques
4.	70 PVL E54	Adaptive Signal Processing	PE	5	3	0	2	4	Digital Signal processing
5.	70 PVL E55	MEMS System Design	PE	5	3	0	2	4	Electronic Circuits

RESEARCH METHODOLOGY (RM)

S.No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C	Prerequisite
1.	70 PIS 001/ 70 PSE 001	Research Methodology and IPR	RM	3	3	0	0	3	Nil

AUDIT COURSES (I/II) (AC)

S.No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C	Prerequisite
1.	70 PAC 001	English for Research Paper Writing	AC	2	2	0	0	0	Nil
2	70 PAC 002	Disaster Management	AC	2	2	0	0	0	Nil

CAREER GUIDANCE COURSES (CG)

S.No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C	Prerequisite
1.	70 PVL 2P2	Term Paper and Seminar	CG	2	0	0	2	0	Nil
2.	70 PVL 3P1	Project Work - Phase I	CG	12	0	0	12	6	Nil
4.	70 PVL 4P1	Project Work - Phase II	CG	24	0	0	24	12	Nil

SUMMARY

S.No.	Category	Credits per semester				Total Credits	Percentage%
		I	II	III	IV		
1.	PC	21	14	3	-	38	52.78
2.	PE	-	6	7	-	13	18.06
3.	RM	3	-	-	-	03	4.17
4.	CG	-	-	6	12	18	25.00
5.	AC	AC I	AC II	-	-	-	-
Total		24	20	16	12	72	100

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SEMESTER I

S.No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C
THEORY								
1.	70 PVL 101	Linear Algebra and Graph Theory	PC	5	3	1	0	4
2.	70 PIS 001/ 70 PSE 001	Research Methodology and IPR	RM	3	3	0	0	3
3.	70 PVL 102	Analog IC Design	PC	3	3	0	0	3
4.	70 PVL 103	Digital IC Design	PC	3	3	0	0	3
5.	70 PVL 104	Advanced Digital System Design	PC	5	3	1	0	4
6.	70 PVL E1*	Professional Elective I	PE	3	3	0	0	3
7.	70 PAC 001	English for Research Paper Writing	AC	2	2	0	0	0
PRACTICALS								
8.	70 PVL 1P1	VLSI Laboratory I	PC	4	0	0	4	2
9.	70 PVL 1P2	Analog IC Design Laboratory	PC	4	0	0	4	2
			TOTAL	**32**	**20**	**2**	**8**	**24**

SEMESTER II

S.No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C
THEORY								
1.	70 PVL 201	Solid State device Modelling and Simulation	PC	3	3	0	0	3
2.	70 PVL 202	VLSI Design Automation	PC	3	3	0	0	3
3.	70 PVL 203	VLSI Testing	PC	3	3	0	0	3
4.	70 PVL 204	ASIC Design	PC	3	3	0	0	3
5.	70 PVL E2*	Professional Elective II	PE	3	3	0	0	3
6.	70 PVL E3*	Professional Elective III	PE	3	3	0	0	3
7.	70 PAC 002	Disaster Management	AC	2	2	0	0	0
PRACTICALS								
8.	70 PVL 2P1	VLSI Laboratory II	PC	4	0	0	4	2
9.	70 PVL 2P2	Term Paper and Seminar	CG	2	0	0	2	0
			TOTAL	**26**	**20**	**0**	**6**	**20**

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SEMESTER III

S.No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C
THEORY								
1.	70 PVL 301	Electronic Packaging	PC	3	3	0	0	3
2.	70 PVL E4*	Professional Elective IV	PE	3	3	0	0	3
3.	70 PVL E5*	Professional Elective V	PE	5	3	0	2	4
PRACTICALS								
4.	70 PVL 3P1	Project Work - Phase I	CG	12	0	0	12	6
			TOTAL	**23**	**9**	**0**	**14**	**16**

SEMESTER IV

S.No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C
PRACTICALS								
1.	70 PVL 4P1	Project Work - Phase II	CG	24	0	0	24	12
			TOTAL	**24**	**0**	**0**	**24**	**12**

TOTAL CREDITS TO BE EARNED FOR THE AWARD OF THE DEGREE: 72

Note: PC-Professional Core Courses, PE-Professional Elective Courses, RM- Research Methodology, CG -Career Guidance Courses, AC- Audit Courses

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M.E. / M.Tech. Degree Programme

SCHEME OF EXAMINATIONS

(For the candidates admitted in 2025-2026)

FIRST SEMESTER

S.No	Course Code	Name of the Course	Duration of Internal Exam	Weightage of Marks			Minimum Marks for Pass in End Semester Exam	
				Continuous Assessment *	End Semester Exam **	Max. Marks	End Semester Exam	Total
THEORY								
1.	70 PVL 101	Linear Algebra and Graph Theory	2	40	60	100	45	100
2.	70 PIS 001/ 70 PSE 001	Research Methodology and IPR	2	40	60	100	45	100
3.	70 PVL 102	Analog IC Design	2	40	60	100	45	100
4.	70 PVL 103	Digital IC Design	2	40	60	100	45	100
5.	70 PVL 104	Advanced Digital System Design	2	40	60	100	45	100
6.	70 PVL E1*	Professional Elective I	2	40	60	100	45	100
7.	70 PAC 001	English for Research Paper Writing	2	100	-	100	-	100
PRACTICAL								
9.	70 PVL 1P1	VLSI Laboratory I	3	60	40	100	45	100
10.	70 PVL 1P2	Analog IC Design Laboratory	3	60	40	100	45	100

* CA evaluation pattern will differ from course to course and for different tests. This will have to be declared in advance to students. The department will put a process in place to ensure that the actual test paper follow the declared pattern.

** End semester Examination will be conducted for maximum marks of 100 and subsequently be reduced to 60 marks for theory End Semester Examination and 40 marks for practical End semester Examination.

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70 PVL 101	Linear Algebra and Graph Theory	Category	L	T	P	Credit
		PC	3	1	0	4

Objectives

- To introduce the concepts of matrix decomposition.
- To know and apply the fundamental concepts in graph theory.
- To learn the model problems using graphs and to solve these problems algorithmically.
- To expose the concepts of modeling and optimization for solving real world problems
- To analyze and solve network models arising from a wide range of applications.

Pre-requisites

- Discrete Mathematics

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Understand the concept of different decomposition	Apply
CO2	Know the basic terminology and some of the theory associated with graphs	Apply
CO3	Formulate graph theoretic models to solve real world problems	Apply
CO4	Explain the linear programming principles and its conversion.	Apply
CO5	Apply CPM and PERT techniques to control project activities and costs	Apply

Mapping with Programme Outcomes

COs	POs					
	1	2	3	4	5	6
CO1	3	3	-	-	2	3
CO2	3	3	-	-	2	3
CO3	3	3	-	-	2	2
CO4	3	3	-	-	2	2
CO5	3	3	-	-	2	2
3 - Strong; 2 - Medium; 1 - Some						

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	14	6	10
Understand	14	6	10
Apply	32	48	80
Analyse	-	-	-
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

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Syllabus

K.S.Rangasamy College of Technology – Autonomous R2025

M.E-VLSI Design

70 PVL 101 - Linear Algebra and Graph Theory

Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
I	3	1	0	60	4	40	60	100

Linear Algebra Introduction – LU Decomposition - QR decomposition – Singular value decomposition – Principal component analysis.	[9]
Graph Theory* Undirected graph — Degree of a vertex - Degree sequence - Sub graphs – Vertex Induced sub graphs - Complement of a graph - Self complementary graphs– Walk Path- Connectivity – Eccentricity – Radius – Diameter - Vertex and edge cuts- Vertex Partition- Independent set - Clique. Digraph — Orientation- Strongly connected Diagraphs- Weekly connected digraphs - Unilaterally connected digraphs- Directed Acyclic graph- Adjacency matrix - Incidence matrix of graphs. Trees - Spanning trees - Matrix tree theorem.	[9]
Graph Algorithms Search algorithms – Depth first search and breadth first search - Spanning tree algorithm-Kruskal's and Prim's shortest path algorithm-Dijkstra's and Floyd-Marshall. Matching-Perfect matching, Bipartite matching. Flow networks - Augmenting path algorithm - Min-cut and max-cut algorithms.	[9]
Linear Programming Formulation of linear programming problem - Graphical method - Simplex method - Two phase method - Big M-method - Duality - Dual simplex method.	[9]
Network Analysis** Introduction - Network and Basic Components - Rules of Network Construction – Critical Path Method – Probability Considerations in PERT - Concept of Project Crashing / Time-Cost trade-off.	[9]
Total Hours: 45 + 15(Tutorial)	**60**

Text Book(s):

1.	Narsingh Deo, Graph Theory with Applications to Engineering and Computer Science, Dover Edition, Mineola, New York, Dover Publications,2016.
2.	KantiSwarup, P.K.Gupta, Man Mohan, ' Operations Research',12th Edition, Sultan Chand & Sons, New Delhi, 2004.

Reference(s):

1.	Gilbert Strang, Introduction to linear algebra, 6th Edition, ANE Books, 2023.
2.	David C. Lay, 'Linear Algebra and its Applications', Pearson Education, 6th edition, 2021.
3.	Hamdy A Taha, 'Operations Research. An Introduction', Pearson Education, New Delhi, 2014.
4.	West D B, 'Introduction To Graph Theory', Pearson Education, New Delhi, 2nd Edition, 2018.

*SDG 4: Quality education.

**SDG 9: Promote inclusive and sustainable industrialization.

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Course Contents and Lecture Schedule		
S. No.	**Topics**	**No. of hours**
1.0	**Linear Algebra**	
1.1	Introduction	1
1.2	LU Decomposition	2
1.3	QR Decomposition	2
1.4	Singular Value Decomposition	2
1.5	Principal Component Analysis	2
1.6	Solving Systems of Linear Equations using the tools of Matrices	1
1.7	Tutorial	2
2.0	**Graph Theory**	
2.1	Undirected graph	1
2.2	Degree of a vertex - Degree sequence	1
2.3	Sub graphs - Vertex induced sub graphs	1
2.4	Complement of a graph - Self complementary graphs	1
2.5	Walk – Path – Connectivity – Eccentricity	1
2.6	Radius – Diameter - Vertex and edge cuts - Vertex partition - Independent set - Clique	1
2.7	Digraph — Orientation – Strongly connected digraphs – Weekly connected digraphs - Unilaterally connected digraphs	2
2.8	Directed acyclic graph. Adjacency matrix - Incidence matrix of graphs. Trees - Spanning trees - Matrix tree theorem	1
2.9	Tutorial	2
3.0	**Graph Algorithms**	
3.1	Search algorithms	1
3.2	Depth first search and breadth first search	2
3.3	Spanning tree algorithm	2
3.4	Kruskal's and Prim's shortest path algorithm	
3.5	Dijkstra's and Floyd-Marshall	2
3.6	Matching	1
3.7	Perfect matching, Bipartite matching, Flow networks	2
3.8	Augmenting path algorithm - Min-cut and max-cut algorithms	
3.9	Tutorial	
4.0	**Linear Programming**	
4.1	Formulation of linear programming problem	1
4.2	Graphical method	1
4.3	Simplex method	2
4.4	Two phase method	1
4.5	Big M-method	2
4.6	Duality	
4.7	Dual simplex method	1
4.8	Tutorial	2
5.0	**Network Analysis**	
5.1	**Introduction**	2

5.2	Network and Basic Components	1
5.3	Rules of Network Construction	2
5.4	Critical Path Method	2
5.5	Probability Considerations in PERT	1
5.6	Concept of Project Crashing / Time-Cost trade-off.	1
5.7	Tutorial	1

Course Designer(s)

Mrs. D.Padmavathi- padmavathi@ksrct.ac.in

70 PIS 001/ 70 PSE 001	Research Methodology and IPR	Category	L	T	P	Credit
		RM	3	0	0	3

Objectives

- To understand the principles of research process.
- To develop knowledge in analytical skills for collection of research data.
- To understand the procedure in the preparation of reports.
- To accomplish basic idea about the process involved in intellectual property rights.
- To enlighten the process of patent filing.

Pre-requisites

- Nil

Course Outcomes

On the successful completion of the course, students will be able to

CO1	To understand the research process and design.	Apply
CO2	To gain the knowledge about sources and collection of research data	Analyse
CO3	To understand the procedure of data analysis, preparation of reports and checking plagiarism	Analyse
CO4	To gain the knowledge on Trade mark and functions of UNESCO in IPR	Apply
CO5	To enlighten the benefits, E-filing and Examinations related to patents	Apply

Mapping with Programme Outcomes

COs	POs					
	1	2	3	4	5	6
CO1	3	3	2	2	2	2
CO2	3	3	2	2	2	2
CO3	3	3	2	2	2	2
CO4	3	3	2	2	2	2
CO5	3	3	2	2	2	2
3 - Strong; 2 - Medium; 1 - Some						

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	10	10	30
Understand	20	20	30
Apply	20	20	30
Analyse	10	10	10
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

Syllabus

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Common to all Branches								
70 PIS 001/70 PSE 001- Research Methodology and IPR								
Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
I	3	0	0	45	3	40	60	100

Research Design* Overview of Research Process and Design- use of Secondary and Exploratory Data to Answer the Research Question, Qualitative Research, Observation Studies, Experiments and Surveys, Selection of the Right Medium and Journal for Publication, Translation of Research	[9]
Data Collection and Sources Measurements, Measurement Scales, Questionnaires and Instruments, Sampling and Methods. Data - Preparing, Exploring, Examining and Displaying.	[9]
Data Analysis and Reporting Overview of Multivariate Analysis, Hypotheses Testing and Measures of Association. Presenting Insights and Findings using Written Reports and Oral Presentation. Checks for Plagiarism, Falsification, Fabrication, and Misrepresentation	[9]
Intellectual Property Rights** Intellectual Property — The Concept of IPR, Evolution and Development of Concept of IPR, IPR Development Process, Trade Secrets, Utility Models, IPR & Bio Diversity, Role of WIPO and WTO in IPR Establishments, Right of Property, Common Rules of IPR Practices, Types and Features of IPR Agreement, Trademark, Functions of UNESCO in IPR Maintenance.	[9]
Patents Patents – Objectives and Benefits of Patent, Concept, Features of Patent, Inventive Step, Specification, Types of Patent Application, Process E-Filling, Examination of Patent, Grant of Patent, Revocation, Equitable Assignments, Licences, Licensing of Related Patents, Patent Agents, Registration of Patent Agents.	[9]
Total Hours	45

Text Book(s):	
1.	David I. Bainbridge, "Intellectual Property", Longman, 9th Edition, 2012.
2.	Cooper Donald R, Schindler Pamela S and Sharma JK, "Business Research Methods", 11th Edition, Tata McGraw Hill Education, 2012.
Reference(s):	
1.	Chawla H S, "Introduction to Intellectual Property Rights", CBS PUB & DIST PVT Limited, INDIA, 2019.
2.	Catherine J. Holland, "Intellectual property: Patents, Trademarks, Copyrights, Trade Secrets", Entrepreneur Press, 2007
3.	David Hunt, Long Nguyen, Matthew Rodgers, "Patent searching: tools & techniques", Wiley, 2007
4.	Arun K. Narasani, Kankanala K.C., Radhakrishnan V., "Indian Patent Law and Practice", Oxford University Press, 2010.
5.	Richard Stim, "Patent, Copyright & Trademark - An Intellectual Property Desk Reference", NOLO Publishers, 2020.
6.	The Institute of Company Secretaries of India, Statutory body under an Act of parliament, "Professional Programme Intellectual Property Rights, Law and practice", September 2013.

*SDG 4: Quality education.

**SDG 9: Industry, Innovation, and Infrastructure.

Course Contents and Lecture Schedule		
S. No.	**Topics**	**No. of hours**
1.0	**Research Design**	
1.1	Overview of Research Process and Design	1
1.2	Use of Secondary and Exploratory Data to Answer the Research Question	2
1.3	Qualitative Research	1
1.4	Observation Studies	1
1.5	Experiments and Surveys	1
1.6	Selection of the Right Medium and Journal for publication	2
1.7	Translation of Research	1
2.0	**Data Collection and Sources**	
2.1	Measurements, Measurement Scales	2
2.2	Questionnaires and Instruments	2
2.3	Sampling and Methods	2
2.4	Data - Preparing, Exploring, Examining and Displaying	3
3	**Data Analysis and Reporting**	
3.1	Overview of Multivariate Analysis	1
3.2	Hypotheses Testing and Measures of Association	2
3.3	Presenting Insights	1
3.4	Findings using Written Reports and Oral Presentation	2
3.5	Checks for Plagiarism	1
3.6	Falsification	1
3.7	Fabrication, and Misrepresentation	1
4	**Intellectual Property Rights**	
4.1	Intellectual Property – The concept of IPR	1
4.2	Evolution and Development of Concept of IPR, IPR Development Process	1
4.3	Trade secrets, Utility Models, IPR & Bio Diversity	2
4.4	Role of WIPO and WTO in IPR Establishments	2
4.5	Right of Property, Common rules of IPR Practices	1
4.6	Types and Features of IPR Agreement, Trademark, Functions of UNESCO in IPR Maintenance	2
5.0	**Patents**	
5.1	Patents – Objectives and Benefits of Patent, Concept, Features of Patent	2
5.2	Inventive step, Specification, Types of Patent Application	2
5.3	Process E-filling, Examination of Patent	1
5.4	Grant of patent, Revocation	1
5.5	Equitable Assignments, Licences, Licensing of Related Patents	2
5.6	Patent agents, Registration of Patent Agents	1

Course Designer(s)

Dr.A.Murugesan – murugesan@ksrct.ac.in

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

70 PVL 102	Analog IC Design	Category	L	T	P	Credit
		PC	3	0	0	3

Objectives

- To develop the ability to analyze, design, and implement analog building blocks using CMOS technology, considering the challenges posed by continued miniaturization and integration in VLSI systems.
- To study the most important building blocks of all CMOS analog IC.
- To provide a comprehensive understanding of the fundamental principles, circuit configurations, and design trade-offs involved in MOS transistor-level design.
- To enable students to understand and analyze the design challenges of single and multistage voltage, current, and differential amplifiers.
- To know the band gap references and temperature independent references.

Pre-requisites

- Courses on Semiconductor Devices and Circuits and Linear IC Applications at UG Level

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Design amplifiers to meet user specifications	Apply
CO2	Analyze the frequency and noise performance of amplifiers	Analyze
CO3	Design and analyze feedback amplifiers and one stage op amps	Apply
CO4	Design and analyze two stage op amps	Apply
CO5	Design and analyze current mirrors and current sinks with MOS devices	Apply

Mapping with Programme Outcomes

COs	POs					
	1	2	3	4	5	6
CO1	3	3	3	2	2	3
CO2	3	3	3	2	2	3
CO3	3	3	3	2	2	3
CO4	3	3	3	2	2	3
CO5	3	3	3	2	2	3
3 - Strong; 2 - Medium; 1 - Some						

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	10	20	10
Understand	20	20	10
Apply	20	20	70
Analyse	10	-	10
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Syllabus

K.S.Rangasamy College of Technology – Autonomous R2025								
M.E-VLSI Design								
70 PVL 102– Analog IC Design								
Semester	**Hours/Week**			**Total Hours**	**Credit**	**Maximum Marks**		
	L	T	P		C	CA	ES	Total
I	3	0	0	45	3	40	60	100

Single Stage Amplifiers* Basic Mos Physics and Equivalent Circuits and Models, CS, CG and Source Follower, Differential Amplifier with Active Load, Cascade and Folded Cascade Configurations with Active Load, Design of Differential and Cascade Amplifiers - to Meet Specified SR, Noise, Gain, BW, ICMR and Power Dissipation, Voltage Swing, High Gain Amplifier Structures	[9]
High Frequency and Noise Characteristics of Amplifiers** Miller Effect, Association of Poles with Nodes, Frequency Response of CS, CG and Source Follower, Cascade and Differential Amplifier Stages, Statistical Characteristics of Noise, Noise in Single Stage Amplifiers, Noise in Differential Amplifiers.	[9]
Feedback and Single Stage Operational Amplifiers Properties and Types of Negative Feedback Circuits, Effect of Loading in Feedback Networks, Operational Amplifier Performance Parameters, Single Stage Op Amps, Two-Stage Op Amps, Input Range Limitations, Gain Boosting, Slew Rate, Power Supply Rejection, Noise in Op Amps.	[9]
Stability and Frequency Compensation of Two Stage Amplifier Analysis of Two Stage Op Amp - Two Stage Op Amp Single Stage CMOS CS as Second Stage and Using Cascade Second Stage, Multiple Systems, Phase Margin, Frequency Compensation, and Compensation of Two Stage Op Amps, Slewing In Two Stage Op Amps, Other Compensation Techniques.	[9]
Bandgap References Current Sinks and Sources, Current Mirrors, Wilson Current Source, Widlar Current Source, Cascade Current Source, Design of High Swing Cascade Sink, Current Amplifiers, Supply Independent Biasing, Temperature Independent References, PTAT and CTAT Current Generation, Constant-GM Biasing	[9]
Total Hours	45

Text Book(s):	
1.	Behzad Razavi, "Design of Analog CMOS Integrated Circuits", Tata McGraw Hill, 2017.
2.	Willey M.C. Sansen, "Analog Design Essentials", Springer, 2010.
Reference(s):	
1.	Grebene, "Bipolar and Mos Analog Integrated Circuit Design", John Wiley & Sons, Inc,2013.
2.	Phillip E.Allen, Douglas R .Holberg, "CMOS Analog Circuit Design", 2nd Edition, Oxford University Press, 2018.
3.	Recorded Lecture Available at http://www.ee.iitm.ac.in/vlsi/courses/ee5320 2021/start
4.	Jacob Baker "CMOS: Circuit Design, Layout, and Simulation", 3rd Edition, Wiley IEEE Press, 2015.

*SDG 9: Industry, Innovation, and Infrastructure
**SDG 12: Responsible Consumption and Production

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Course Contents and Lecture Schedule		
S. No.	**Topics**	**No. of hours**
1	**Single Stage Amplifiers**	
1.1	Basic MOS Physics and Equivalent Circuits and Models	1
1.2	CS, CG and Source Follower	1
1.3	Differential Amplifier with Active Load	1
1.4	Cascade and Folded Cascade Configurations with Active Load	1
1.5	Design of Differential and Cascade Amplifiers	1
1.6	Slew Rate, Noise, Gain, Bandwidth	1
1.7	ICMR and Power Dissipation	1
1.8	Voltage Swing	1
1.9	High Gain Amplifier Structures	1
2	**High Frequency and Noise Characteristics of Amplifiers**	
2.1	Miller effect	1
2.2	Association of Poles with Nodes	1
2.3	Frequency Response of CS, CG	1
2.4	Frequency Response of Source Follower	1
2.5	Cascade Amplifier Stages	1
2.6	Differential Amplifier Stages	1
2.7	Statistical Characteristics of Noise	1
2.8	Noise in Single Stage Amplifiers	1
2.9	Noise in Differential Amplifiers	1
3	**Feedback and Single Stage Operational Amplifiers**	
3.1	Properties and Types of Negative Feedback Circuits	1
3.2	Effect of loading in Feedback Networks	1
3.3	Operational Amplifier Performance Parameters	1
3.4	Single stage Op Amps	1
3.5	Two stage Op Amps	1
3.6	Input range Limitations and Gain Boosting	1
3.7	Slew Rate, Power Supply Rejection	1
3.8	Noise in Op Amps	1
4	**Stability and Frequency Compensation of Two Stage Amplifier**	
4.1	Analysis of Two Stage Op Amp	1
4.2	Two Stage Op Amp Single Stage CMOS CS as Second Stage and Using Cascade Second Stage	2
4.3	Multiple Systems	1
4.4	Phase Margin	1
4.5	Frequency Compensation	1
4.6	Compensation of Two Stage Op Amps	1
4.7	Slewing in Two Stage Op Amps	1
4.8	Other Compensation Techniques	1
5	**Bandgap References**	
5.1	Current sinks, Sources and Current Mirrors	1
5.2	Wilson current Source, Widlar Current Source	1
5.3	Cascade Current Source	1
5.4	Design of High Swing Cascade Sink	1
5.5	Current Amplifiers	1

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5.6	Supply Independent Biasing	1
5.7	Temperature Independent References	1
5.8	PTAT and CTAT Current Generation	1
5.9	Constant-GM Biasing	1

Course Designer(s)

Saravanan S - saravanan.s@ksrct.ac.in

70 PVL 103	Digital IC Design	Category	L	T	P	Credit
		PC	3	0	0	3

Objectives

- To introduce the fundamentals of MOS circuit design, covering CMOS inverters, power dissipation, and interconnect effects.
- To explore combinational and sequential CMOS logic design techniques and their influence on circuit performance.
- To develop arithmetic building blocks, including adders, multipliers, and comparators, while considering power-speed trade-offs.
- To examine timing-related challenges in VLSI circuits and study synchronizers, metastability, and self-timed design approaches.
- To provide hands-on experience in designing and optimizing data path structures for digital processor architectures

Pre-requisites

- Digital logic design, VLSI Design

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Explain MOS circuit design principles, including CMOS inverter characteristics, power dissipation, and interconnect effects, lithography	Apply
CO2	Analyze different combinational and sequential CMOS logic design techniques and their impact on circuit performance.	Analyze
CO3	Design arithmetic building blocks such as adders, multipliers, and comparators with optimized power-speed trade-offs.	Apply
CO4	Evaluate timing issues in VLSI circuits, including synchronizers, metastability, and self-timed circuit designs.	Apply
CO5	Demonstrate proficiency in implementing data path structures and optimizing digital processor architectures.	Apply

Mapping with Programme Outcomes

COs	POs					
	1	2	3	4	5	6
CO1	3	3	3	2	2	3
CO2	3	3	3	2	2	3
CO3	3	3	3	2	2	3
CO4	3	3	3	2	2	3
CO5	3	3	3	2	2	3
3 - Strong; 2 - Medium; 1 - Some						

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	10	20	30
Understand	20	20	10
Apply	20	20	30
Analyse	10	-	30
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Syllabus

K.S.Rangasamy College of Technology – Autonomous R2025								
M.E-VLSI Design								
70 PVL 103– Digital IC Design								
Semester	**Hours/Week**			**Total Hours**	**Credit**	**Maximum Marks**		
	L	T	P		C	CA	ES	Total
I	3	0	0	45	3	40	60	100

MOS Circuit Design Process* Overview of VLSI Design Flow, MOSFET Enhancement Transistors and MOS Device Physics- CMOS Inverter Characteristics, DC Transfer Curves and Switching Behavior - Power Dissipation, Photolithography, E-beam lithography and newer lithography techniques for VLSI/ULSI;Mask generation	[9]
Combinational CMOS Logic Design Static and Complementary CMOS Logic Design Principles - Pass Transistor Logic and Transmission Gate Implementation - Dynamic CMOS Design Techniques and Performance Considerations - Signal Integrity Issues, Including Noise, Glitches and Charge Sharing Effects	[9]
Sequential CMOS Logic Design Design of Static and Dynamic Latches and Registers - Pulse-Triggered and Sense Amplifier-Based Register Architectures - Pipelining Techniques for High-Speed Sequential Circuits - Non-Bistable Sequential Circuit Concepts and Applications.	[9]
Timing Issues IN VLSI Circuits Classification of Timing in Digital Systems and Synchronization Challenges - Timing Constraints and Issues in Synchronous Circuit Design - Self-timed Circuit Design Methodologies for Asynchronous Systems - Synchronizers and Arbiters for Resolving Metastability and Timing Conflicts.	[9]
Design of Arithmetic Building Blocks** Datapath Design in Digital Processor Architectures - Design of Binary Adders, Multipliers and Shifters – Array based subsystems based on CMOS and FinFET design:SRAM, DRAM,ROM.	[9]
Total Hours	45

Text Book(s):	
1.	Jan M Rabaey, Anantha Chandrakasan and Borivoje Nikolic, "Digital Integrated Circuits - A Design Perspective", 2nd Edition, Prentice Hall, 2018.
2.	John P.Uyemura, "Introduction to VLSI Circuits and Systems", John Wiley & Sons,
3.	**Chris A. Mack**," Fundamental Principles of Optical Lithography: The Science of Microfabrication", 2nd Edition,John Wiley & Sons Ltd, 2017
Reference(s):	
1.	Neil H. E. Weste and Kamran Eshraghian, "Principles of CMOS VLSI Design - A Systems Perspective", 2nd Edition, Pearson Education, 2010.
2.	Kamran Eshraghian, Douglas A. Pucknell, "Essentials of VLSI Circuits and Systems", Prentice Hall, 2011
3.	C.Mead and L.Conway, "Introduction to VLSI Systems", Addison Wesley, 1999
4.	Kang, "CMOS Digital Integrated Circuits", McGraw Hill, 2012.

* SDG 7: Affordable and Clean Energy
** SDG 9: Industry, Innovation, and Infrastructure

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Course Contents and Lecture Schedule

S. No.	Topics	No. of hours
1	**MOS circuit design process**	
1.1	Overview of VLSI Design Flow	1
1.2	MOSFET Enhancement Transistors	1
1.3	MOS Device Physics	1
1.4	CMOS Inverter Characteristics	1
1.5	DC Transfer Curves and Switching Behavior	1
1.6	Power Dissipation	1
1.7	Photolithography	1
1.8	E-beam lithography and newer lithography techniques for VLSI/ULSI	1
1.9	Mask generation	1
2	**Combinational CMOS Logic Design**	
2.1	Static CMOS Logic Design Principles	1
2.2	Complementary CMOS Logic Design	1
2.3	Pass Transistor Logic	1
2.4	Transmission Gate Implementation	1
2.5	Dynamic CMOS Design Techniques and Performance Considerations	1
2.6	Signal Integrity Issues	1
2.7	Noise	1
2.8	Glitches	1
2.9	Charge Sharing Effects	1
3	**Sequential CMOS Logic Design**	
3.1	Design of Static and Dynamic Latches and Registers	2
3.2	Pulse-Triggered Architectures	1
3.3	Sense Amplifier Based Register Architectures	2
3.4	Pipelining Techniques for High-Speed Sequential Circuits	2
3.5	Non-Bistable Sequential Circuit Concepts and Applications	2
4	**Timing Issues In VLSI Circuits**	
4.1	Classification of Timing in Digital Systems	1
4.2	Synchronization Challenges	2
4.3	Timing Constraints and Issues in Synchronous Circuit Design	2
4.4	Self-timed Circuit Design Methodologies for Asynchronous Systems	2
4.5	Synchronizers and Arbiters for Resolving Metastability and Timing Conflicts	2
5	**Design of Arithmetic Building Blocks**	
5.1	Datapath Design in Digital Processor Architectures	1
5.2	Design of Binary Adders	2
5.3	Design of Multipliers	1
5.4	Design of Shifters	1
5.5	Array based subsystems based on CMOS and FinFET design	1
5.6	SRAM,	1
5.7	DRAM, ROM.	2

Course Designer(s)

Dr. D. Mugilan - mugilan@ksrct.ac.in

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

70 PVL 104	Advanced Digital System Design	Category	L	T	P	Credit
		PC	3	1	0	4

Objectives

- To design asynchronous sequential circuits
- To identify hazards in asynchronous sequential circuits
- To study the fault testing procedure for digital circuits.
- To learn about the architecture of programmable devices.
- To design and implement digital circuits using programming tools.

Pre-requisites

- Digital Logic Design

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Describe synchronous sequential circuits.	Understand
CO2	Analyze hazards in asynchronous sequential circuits.	Apply
CO3	Discuss the testing procedure for combinational circuit and PLA.	Analyse
CO4	Design PLD and ROM.	Analyse
CO5	Design and use programming tools for implementing digital circuits	Analyse

Mapping with Programme Outcomes

COs	POs					
	1	2	3	4	5	6
CO1	3	3	3	3	3	3
CO2	3	3	3	3	3	3
CO3	3	3	3	3	3	3
CO4	3	3	3	3	3	3
CO5	3	3	3	3	3	3
3 - Strong; 2 - Medium; 1 - Some						

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	20	10	30
Understand	20	20	30
Apply	20	20	30
Analyse	-	10	10
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Syllabus

K.S.Rangasamy College of Technology – Autonomous R2025								
M.E-VLSI Design								
70 PVL 104- Advanced Digital System Design								
Semester	**Hours/Week**			**Total Hours**	**Credit**	**Maximum Marks**		
	L	T	P		C	CA	ES	Total
I	3	1	0	60	4	40	60	100

Sequential Circuit Design* Analysis of Clocked Synchronous Sequential Circuits and Modelling- State Diagram, State Table, State Table Assignment and Reduction-Design of Synchronous Sequential Circuits Design of Iterative Circuits-ASM Chart.	[9]
Asynchronous Sequential Circuit Design Analysis of Asynchronous Sequential Circuit — Flow Table Reduction-Races-State Assignment- Transition Table and Problems in Transition Table- Design of Asynchronous Sequential Circuit - Static, Dynamic and Essential hazards – Mixed Operating Mode Asynchronous Circuits – Designing Vending Machine Controller.	[9]
Fault Diagnosis and Testability Algorithms** Fault Table Method-Path Sensitization Method — Boolean Difference Method - Kohavi Algorithm D Algorithm —Tolerance Techniques – The Compact Algorithm – Fault in PLA – Test Generation - DFT Schemes – Built in Self Test	[9]
Synchronous Design Using Programmable Devices and System Design Using VHDL Programmable Logic Devices — Designing a Synchronous Sequential Circuit using PLA/ PAL Computer Aided Design — Realization of Finite State Machine using PLD.FPGA — Xilinx FPGA - Xilinx 2000 - Xilinx 3000 - Xilinx 4000. VHDL Description of Combinational Circuits and sequential circuit. VHDL Operators — Compilation and Simulation of VHDL Code — Modeling using VHDL.	[9]
Timing Analysis ROM timings - Static RAM timing - Synchronous Static RAM and it's timing - Dynamic RAM timing, Complex Programmable Logic Devices - Logic Analyzer Basic Architecture - Internal structure - Data display - Setup and Control - Clocking and Sampling	[9]
Total Hours: 45 + 15(Tutorial)	60

Text Book(s):	
1.	Donald G. Givone, "Digital principles and Design", Tata McGraw Hill, 2016.
2.	John M Yarbrough, 'Digital Logic applications and Design', Thomson Learning, 2017.
Reference(s):	
1.	Nripendra N Biswas, "Logic Design Theory", Prentice Hall of India Private Ltd., 2016.
2.	Charles H. Roth Jr., 'Digital System Design using VHDL', Thomson Learning, 2016.
3.	Wakerly J.F, 'Digital Design Principles and Practices', 4 Edition, Pearson Education, 2017.
4.	Wakerly J.F, 'Digital Design: Principles and Practices', 3 Edition, Pearson Education, 2016.

* SDG 4: Quality Education
** SDG 17: Partnerships for the Goals

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Course Contents and Lecture Schedule

S. No.	Topics	No. of hours
1	**Sequential Circuit Design**	
1.1	Analysis of Clocked Synchronous Sequential Circuits and Modelling	2
1.2	State Diagram	1
1.3	State Table, State Table Assignment and Reduction	1
1.4	Design of Synchronous Sequential Circuits	1
1.5	Design of Iterative Circuits	1
1.6	ASM Chart	2
2	**Asynchronous Sequential Circuit Design**	
2.1	Analysis of Asynchronous Sequential Circuit	1
2.2	Flow Table Reduction	1
2.3	Races-State Assignment	1
2.4	Transition Table and Problems in Transition Table.	1
2.5	Design of Asynchronous Sequential	1
2.6	Circuit - Static, Dynamic and Essential	1
2.7	Hazards	1
2.8	Mixed Operating Mode Asynchronous Circuits	1
2.9	Designing Vending Machine Controller	1
3	**Fault Diagnosis and Testability Algorithms**	
3.1	Fault Table Method	1
3.2	Path Sensitization Method	1
3.3	Boolean Difference Method	1
3.4	Kohavi Algorithm D Algorithm	1
3.5	Tolerance Techniques	1
3.6	The Compact Algorithm	1
3.7	Fault in PLA	1
3.8	Test Generation	1
3.9	DFT Schemes – Built in Self Test	1
4	**Synchronous Design Using Programmable Devices and System Design Using VHDL**	
4.1	Programmable Logic Devices	1
4.2	Designing a Synchronous Sequential Circuit using PLA/ PAL Computer Aided Design	2
4.3	Realization of Finite State Machine using PLD.FPGA	1
4.4	Xilinx FPGA	1
4.5	Xilinx 2000 - Xilinx 3000 - Xilinx 4000.	1
4.6	VHDL Description of Combinational Circuits and Sequential Circuit.	1
4.7	VHDL Operators	1
4.8	Compilation and Simulation of VHDL Code – Modeling using VHDL	1
5	**Timing Analysis**	
5.1	ROM timings	1
5.2	Static RAM timing	1
5.3	Synchronous Static RAM and it's timing	1
5.4	Dynamic RAM timing	1
5.5	Complex Programmable Logic Devices	1
5.6	Logic Analyzer Basic Architecture	1
5.7	Internal Structure	1

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

5.8	Data Display	1

5.9	Setup and Control - Clocking and Sampling	1

Course Designer(s)

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Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

70 PVL E11	System Design with FPGA	Category	L	T	P	Credit
		PE	3	0	0	3

Objectives

- To identify the different types of programming elements, programmable logic blocks, programmable input-output blocks and programmable interconnects of various types of FPGAs
- To understand the steps involved in synthesis, simulation, and testing of systems
- To design and implement circuits, subsystem and system using FPGA and I/O boards

Pre-requisites

- Digital System Design

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Acquire the knowledge on basic concepts of FPGA and its structures	Understand
CO2	Describe the steps involved in synthesis, simulation, and testing of systems	Understand
CO3	Design combinational and arithmetic circuits using FPGA board	Create
CO4	Design memories and DCTQ processor	Create
CO5	Design real time applications using FPGA board	Create

Mapping with Programme Outcomes

COs	POs					
	1	2	3	4	5	6
CO1	2	1	1	-	2	3
CO2	2	1	1	1	2	3
CO3	3	2	2	2	2	3
CO4	3	2	2	2	2	3
CO5	3	2	2	2	2	3
3 - Strong; 2 - Medium; 1 - Some						

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	20	10	10
Understand	40	10	10
Apply	-	20	20
Analyse	-	-	30
Evaluate	-	-	-
Create	-	20	30
Total	60	60	100

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Syllabus

K.S.Rangasamy College of Technology – Autonomous R2025								
M.E-VLSI Design								
70 PVL E11– System Design with FPGA								
Semester	**Hours/Week**			**Total Hours**	**Credit**	**Maximum Marks**		
	L	T	P		C	CA	ES	Total
I	3	0	0	45	3	40	60	100

FPGA Architectures* Basic Concepts - Digital Design and FPGAs - The Role of FPGAs - FPGA Types - FPGAs vs Custom VLSI - FPGA-Based System Design - Goals and Techniques - Hierarchical Design - Design Abstraction- Methodologies. FPGA Basics: Components of an FPGA - Programming Technology - Antifuse Technology - Logic Circuit Representation of FPGA. FPGA Structure: Logic Block - Logic Cluster — Adaptive LUT - Routing Part - Switch Block - Connection Block - I/O Block - DSP Block - Hard Macros - Embedded Memory - Configuration Chain - PLL and DLL	[9]
FPGA Design Flow Design Flow and Design Tools: Design Flow - Design Flow by HDL - HLS Design - IP-Based Design - Design with Processor. Design Methodology: FPGA Design Flow - Technology Mapping - Clustering - Place and Route - Low Power Design Tools. Simulation and Synthesis Concepts - Place and Route – Technology Mapping.	[9]
FPGA Based Subsystem Design **Combinational Circuits**: Basic Gates - Majority Logic and Concatenation - Shift Operations - Multiplexers - Demultiplexer - Full Adder - Magnitude Comparator. Sequential Circuits: D Flip-flop - Registers - Shift Registers - Counters - Finite State Machines - Pattern Sequence Detector. Arithmetic Circuit Designs: Digital Pipelining - Partitioning of a Design - Signed Adder Design - Multiplier Design.	[9]
FPGA Based System Design** Design of Memories: On-chip Dual Address ROM Design - Single Address ROM Design - On Chip Dual RAM Design - External Memory Controller Design. System Designs: Discrete Cosine Transform and Quantization Processor - FOSS Motion Estimation Processor - DCTQ Processor	[9]
FPGA Based Project Design Project Designs: Traffic Light Controller - Real Time Clock - Digital Signal Processor - PCI Bus Arbiter - DCTQ Processor - Electrostatic Precipitator Controller - JPEG/H.263/MPEG 1/ MPEG 2 Codec.	[9]
Total Hours	45

Text Book(s):	
1.	Wayne Wolf, “FPGA-Based System Design”, PTR Prentice Hall, 2004
2.	Hideharu Amano, “Principles and Structures of FPGAs”, Springer, 2018
Reference(s):	
1.	Ramachandran S, “Digital VLSI Systems Design: A Design Manual for Implementation of Projects on FPGAs and ASICs Using Verilog”, Springer, 2007
2.	Peter R. Wilson, “Design Recipes for FPGAs”, Springer, 2008
3.	Sanjay Churiwala, “Designing with Xilinx FPGAs Using Vivado”, Springer, 2017

* SDG 9 - Industry, Innovation, and Infrastructure
** SDG 12 - Responsible Consumption and Production

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Course Contents and Lecture Schedule

S. No.	Topics	No. of hours
1	**FPGA Architectures**	
1.1	Basic Concepts - Digital Design and FPGAs	1
1.2	The Role of FPGAs - FPGA Types - FPGAs vs. Custom VLSI	1
1.3	FPGA-Based System Design - Goals and Techniques - Hierarchical Design - Design Abstraction- Methodologies	1
1.4	Components of an FPGA - Programming Technology - Antifuse Technology	1
1.5	Logic Circuit Representation of FPGA, Logic Block - Logic Cluster	1
1.6	Adaptive LUT - Routing Part - Switch Block - Connection Block	1
1.7	I/O Block - DSP Block - Hard Macros	1
1.8	Embedded Memory	1
1.9	Configuration Chain - PLL and DLL	1
2	**FPGA Design Flow**	
2.1	Design Flow - Design Flow by HDL	1
2.2	HLS Design - IP-Based Design	1
2.3	Design with Processor. Design Methodology	1
2.4	Technology Mapping – Clustering	1
2.5	Place and Route - Low Power Design Tools	2
2.6	Simulation and Synthesis Concepts	2
2.7	Place and Route – Technology Mapping	1
3	**FPGA Based Subsystem Design**	
3.1	Basic Gates - Majority Logic and Concatenation	1
3.2	Shift Operations - Multiplexers - Demultiplexer - Full Adder	1
3.3	Magnitude Comparator, D Flip-flop	2
3.4	Registers - Shift Registers	1
3.5	Counters - Finite State Machines	1
3.6	Pattern Sequence Detector	1
3.7	Digital Pipelining - Partitioning of a Design	1
3.8	Signed Adder Design - Multiplier Design	
4	**FPGA Based System Design**	
4.1	On-chip Dual Address ROM Design	1
4.2	Single Address ROM Design	2
4.3	On Chip Dual RAM Design	1
4.4	External Memory Controller Design	1
4.5	Discrete Cosine Transform and Quantization Processor	2
4.6	FOSS Motion Estimation Processor	1
4.7	DCTQ Processor	1
5	**FPGA Based Project Design**	
5.1	Project Designs: Traffic Light Controller	1
5.2	Real Time Clock	1
5.3	Digital Signal Processor	1
5.4	PCI Bus Arbiter	1
5.5	DCTQ Processor	1
5.6	Electrostatic Precipitator Controller	1
5.7	JPEG	1

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Approved in Academic Council Meeting held on 19/07/2025

5.8	H.263	1
5.9	MPEG 1/ MPEG 2 Codec	1

Course Designer(s)

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Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

70 PVL E12	Advanced Computer Architecture	Category	L	T	P	Credit
		PE	3	0	0	3

Objectives

- To impart basic concepts of computer architecture and theory of parallelism
- To explain key skills of constructing cost-effective computer systems.
- To familiarize program and network properties
- To help students in understanding various architectures and hardware technologies
- To facilitate students in analyzing scalability and performance issues in various architectures.

Pre-requisites

- Nil

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Describe the principles of computer design.	Understand
CO2	Compare the performance of different architectures	Understand
CO3	Improve application performance for different CPU architectures.	Understand
CO4	Develop applications for high performance computing systems	Apply
CO5	Describe the scalable and architecture data flow	Understand

Mapping with Programme Outcomes

COs	POs					
	1	2	3	4	5	6
CO1	3	3	-	-	-	3
CO2	3	2	-	2	-	3
CO3	3	3	-	-	-	3
CO4	3	2	-	-	-	3
CO5	3	3	-	3	-	3
3 - Strong; 2 - Medium; 1 - Some						

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	30	15	30
Understand	30	35	40
Apply	-	10	30
Analyse	-	-	-
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Syllabus

K.S.Rangasamy College of Technology – Autonomous R2025

M.E-VLSI Design

70 PVL E12- Advanced Computer Architecture

Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
I	3	0	0	45	3	40	60	100

Theory of Parallelism State of computing, Multiprocessors and Multi computers, Multi vector and SIMD computers. PRAM and VLSI models, Architectural Development tracks. Program and Network properties.	[9]
Principles of Performance and Hardware Technology Performance Metrics and Measures, Parallel Processing Applications, Speedup Performance Laws, Scalability Analysis and Approaches, Advanced Processor Technology, Superscalar and Vector Processors, Memory Hierarchy Technology, Virtual Memory Technology.	[9]
Bus Cache and Shared Memory* Bus Systems, Cache Memory Organizations, Shared Memory Organizations. **Pipelining and Superscalar Techniques** Linear Pipeline Processors, Nonlinear Pipeline Processors, Instruction Pipeline Design, Arithmetic Pipeline Design.	[9]
Parallel and Scalable Architectures Multiprocessor System Interconnects, Cache Coherence and Synchronization Mechanisms, Message-Passing Mechanisms, Vector Processing Principles, Multifactor Multiprocessors, implementation Models	[9]
Scalable, Multithreaded, and Dataflow Architectures Inter processor Communications, Latency hiding technique Case study: CM 5	[9]
Total Hours	**45**

Text Book(s):

1.	Kai Hwang, Naresh Jotwani, "Advanced Computer Architecture- Parallelism, Scalability, Programmability", 2nd Edition, Tata McGraw Hill.
2.	C. Hamacher, Z. Vranesic and S. Zaky, Computer Organization, McGraw-Hill, 5th Edition,2002, ISBN: 0072320869

Reference(s):

1.	William Stallings, "Computer Organization and Architecture - Designing for performance", Pearson, 2017
2.	Richard Y Kain, "Advanced Computer Architecture: A Systems Design Approach", PHI.
3.	Andrew S. Tanenbaum, "Structured Computer Organization", Prentice Hall, 6th Edition, 2012, ISBN: 978-0132916523

* SDG 9- Industry, Innovation, and Infrastructure

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Course Contents and Lecture Schedule

S. No.	Topics	No. of hours
1	**Theory of Parallelism**	
1.1	State of computing, Multiprocessors and Multi computers	2
1.2	Multi vector and SIMD computers	2
1.3	PRAM and VLSI models	1
1.4	Architectural Development tracks	2
1.5	Program and Network properties	2
2	**Principles of Performance and Hardware Technology**	
2.1	Performance Metrics and Measures	1
2.2	Parallel Processing Applications	1
2.3	Speedup Performance Laws	1
2.4	Scalability Analysis and Approaches	2
2.5	Advanced Processor Technology	1
2.6	Superscalar and Vector Processors	1
2.7	Memory Hierarchy Technology	1
2.8	Virtual Memory Technology	1
3	**Bus Cache and Shared Memory**	
3.1	Bus Systems	1
3.2	Cache Memory Organizations	1
3.3	Shared Memory Organizations	1
3.4	Linear Pipeline Processors	1
3.5	Nonlinear Pipeline Processors	1
3.6	Instruction Pipeline Design	2
3.7	Arithmetic Pipeline Design	1
4	**Parallel and Scalable Architectures**	
4.1	Multiprocessor System Interconnects	1
4.2	Cache Coherence and Synchronization Mechanisms	1
4.3	Message-Passing Mechanisms	2
4.5	Vector Processing Principles	2
4.6	Multifactor Multiprocessors	1
4.7	implementation Models	2
5	**Scalable, Multithreaded and Dataflow Architectures**	
5.1	Interprocessor Communications	3
5.2	Latency hiding technique	3
5.3	Case study: CM 5	3

Course Designer(s)

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Passed in BoS Meeting held on 13/06/2025
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70 PVL E13	VLSI Digital Signal Processing	Category	L	T	P	Credit
		PE	3	0	0	3

Objectives

- To learn the different types of Digital filters.
- To know the concepts of iteration bound.
- To learn the various transformations include retiming folding and unfolding.
- To acquire knowledge in pipelining and parallel processing.
- To learn the concepts of fast convolution and algorithmic strength reduction.

Pre-requisites

- Nil

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Design FIR and IIR digital filters	Apply
CO2	Apply various algorithms to compute iteration bound of DSP system	Apply
CO3	Describe the concepts of pipelining and parallel processing of FIR digital filters.	Apply
CO4	Design a high-level architectural transformation which includes retiming folding and unfolding	Analyse
CO5	Describe the techniques of fast convolution algorithm and architecture strength reduction in filters.	Apply

Mapping with Programme Outcomes

COs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	3	3	3	3
CO2	3	3	3	2	2	3
CO3	3	3	3	3	3	3
CO4	3	3	3	2	2	3
CO5	3	3	3	2	3	3
3 – Strong; 2 – Medium; 1 - Some						

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	20	15	30
Understand	20	15	30
Apply	20	10	20
Analyse	-	20	20
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Syllabus

K.S. Rangasamy College of Technology – Autonomous R 2025								
M.E-VLSI Design								
70 PVL E13- VLSI Digital Signal Processing								
Semester	**Hours / Week**			**Total Hours**	**Credit**	**Maximum Marks**		
	L	T	P		C	CA	ES	Total
I	3	0	0	45	3	40	60	100

Realization of Digital Filters FIR filter design - IIR filter design - Direct form I, II, Cascade, Parallel, Ladder - Lattice filters.	[9]
Iteration Bound Introduction, Data Flow Graph Representations, Loop Bound and Iteration Bound, Algorithms for Computing Iteration Bound, Iteration Bound of Multirate Data - Flow Graphs	[9]
Pipelining and Parallel Processing Introduction - Pipelining of FIR Digital Filters - Parallel Processing - Pipelining and Parallel Processing for Low Power.	[9]
Transformations RETIMING- Introduction - Definitions and Properties - Solving System of Inequalities - Retiming Techniques. UNFOLDING: Introduction - An Algorithm for Unfolding - Properties of Unfolding - Critical Path, Unfolding and Retiming - Application of Unfolding. FOLDING: Introduction - Folding Transformation - Register Minimization Techniques - Register Minimization in Folded Architectures.	[9]
Fast Convolution Cook - Toom Algorithm –Modified Cook - Toom Algorithm Winograd Algorithm- Modified Winograd Algorithm, Algorithmic Strength Reduction in Filters and Transforms-Parallel FIR Filters, Parallel Architectures for Rank-Order Filter.	[9]
	Total Hours: 45

Text book(s):	
1	KeshabKParhi, “VLSI Digital Signal Processing Systems Design and Implementation”, Wiley - Inter science, 2018.
2	John G Proakis and Dimitris G Manolakis, “Digital signal processing – Principles, Algorithms and Applications”, Pearson, 2015.
Reference(s):	
1	Kuang S.Y, White house H.J, T. Kailath, “VLSI and Modern Signal Processing”, Prentice Hall of India Private Ltd., 2013.
2	Uwe Meyer Baese, “Digital Signal Processing with Field Programmable Gate Arrays”, Springer, 2014.
3	Lonnie C Ludeman, “Fundamentals of Digital Signal Processing”, Wiley India (P) Ltd., 2020.
4	Peter Pirsch “Architectures for Digital Signal Processing”, Wiley India (P) Ltd., 2019.

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Course Contents and Lecture Schedule

S.No	Topic	No. of Hours
1	**Realization of Digital Filters**	
1.1	FIR Filter Design	1
1.2	IIR Filter Design	1
1.3	Direct form I Realization	1
1.4	Direct form II Realization	1
1.5	Cascade Realization	1
1.6	Parallel Realization	1
1.7	Ladder form Realization	1
1.8	Lattice Filters	2
2	**Iteration Bound**	
2.1	Introduction	1
2.2	Data flow Graph Representations	2
2.3	Loop Bound and Iteration Bound	2
2.4	Algorithms for Computing iteration Bound	2
2.5	Iteration Bound of Multirate Data - Flow Graphs	2
3	**Pipelining and Parallel Processing**	
3.1	Introduction	1
3.2	Pipelining of FIR Digital filters	2
3.3	Parallel Processing	2
3.4	Pipelining for Low power	2
3.5	Parallel Processing for Low Power	2
4	**Transformations**	
4.1	RETIMING- Introduction - Definitions and Properties	1
4.2	Solving System of Inequalities, Retiming Techniques	1
4.3	UNFOLDING: Introduction, An Algorithm for Unfolding	1
4.4	Properties of unfolding, Critical path, Unfolding and Retiming	1

4.5	Application of Unfolding	1
4.6	Folding: Introduction	1
4.7	Folding Transformation	1
4.8	Register Minimization Techniques	1
4.9	Register Minimization in Folded Architectures	1
5	**Fast Convolution**	
5.1	Introduction	1
5.2	Cook - Toom Algorithm	1
5.3	Modified Cook - Toom Algorithm	1
5.4	Winograd Algorithm	1
5.5	Modified Winograd Algorithm	1
5.6	Algorithmic Strength Reduction in Filters and Transforms	2
5.7	Parallel FIR Filters	1
5.8	Parallel Architectures for Rank-order Filter.	1

Course Designers

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Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

70 PVL E14	Machine Learning in VLSI Design	Category	L	T	P	Credit
		PE	3	0	0	3

Objectives

- To study the concept of machine learning, and performance improvement through data pre-processing.
- To explain the various supervised learning algorithms.
- To learn the different techniques of Unsupervised Learning and Ensemble Methods.
- To learn the VLSI testing process including off-chip and on-chip testing techniques.
- To explore the machine learning techniques in various stages of VLSI design and manufacturing.

Pre-requisites

- Nil

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Describe the concept of machine learning, data preprocess, train and evaluate machine learning models.	Apply
CO2	Apply the linear and nonlinear machine learning models.	Apply
CO3	Apply the different techniques of Unsupervised Learning and Ensemble Methods.	Apply
CO4	Apply VLSI testing methods and leverage ML techniques to optimize verification for power, performance.	Apply
CO5	Apply machine learning techniques in various stages of VLSI design and manufacturing to enhance performance.	Apply

Mapping with Programme Outcomes

COs	POs					
	1	2	3	4	5	6
CO1	3	3	2	3	-	3
CO2	3	3	3	3	-	3
CO3	3	3	3	3	3	3
CO4	3	-	2	3	2	3
CO5	3	3	3	3	3	3
3 - Strong; 2 - Medium; 1 - Some						

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	12	10	20
Understand	28	30	50
Apply	20	20	20
Analyse	-	-	10
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Syllabus

K.S.Rangasamy College of Technology – Autonomous R2025								
M.E-VLSI Design								
70 PVL E14 – Machine Learning in VLSI Design								
Semester	Hours / Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
I	3	0	0	45	3	40	60	100

Machine Learning –Pre-processing to Performance Machine Learning - Types - Pre-processing - Feature Engineering - Feature transformation - Feature Subset Selection, Feature Embedding - Training a Mode - Preparing to Model - Data, Modelling and Evaluation - Evaluating Performance of a Model - Improving Performance.	[9]
Supervised Learning Linear Regression - Logistic Regression - Decision Tree - Rule-Based Classification, Support Vector Machines - Radial Basis Functions - Neural and Belief Networks - Perceptron - Multi-Layer feed Forward Network - Naïve Bayes Classifier.	[9]
Unsupervised Learning and Ensemble Methods K-means Clustering - Hierarchical Methods — Fuzzy Clustering - Principal Component Analysis (PCA) - Linear Discriminant Analysis (LDA), Partitioning Methods - Density Based Methods DBSCAN - Finding Patterns using Association Rules - Finding Patterns using Association rules- Markov Chain Monte Carlo Methods - Hidden Markov Model- Bagging and Boosting	[9]
Machine Learning - VLSI Test and Verification VLSI Testing Process - Off-Chip Testing-On-Chip Testing, Combinational Circuit Testing, Sequential Circuit Testing - ML Advantages-Verification Process - Time-Saving - 3Ps (Power, Performance, Price), Electronic Design Automation (EDA)	[9]
Applications of ML ML in Manufacturing Process, Reducing Maintenance Costs and Improving Reliability, Enhancing New Design - Mask Synthesis - ML in VLSI Functional Verification- ML in Physical Design - Floor Planning and Placement Optimization - Routing Optimization - Case Studies - Power Estimation using Random Forest.	[9]
Total Hours :	**45**

Text Book(s):

1. Ethem Alpaydm, "Introduction to Machine Learning", 4th Edition, The MIT Press, Cambridge, 2020.
2. Anuradha Srinivasaraghavan, Vincy Joseph, “Machine Learning”, 1st Edition, Wiley, 2019.
3. Roger Woods, John McAllister, Gaye Lightbody, Ying Yi, “FPGA Based Implementation of Signal Processing Systems”, John Wile, 2017.

Reference(s):

1. E. Alpaydin, Introduction to Machine Learning, 3rd Edition, Prentice Hall (India) 2015.
2. Tom M Mitchell, “Machine Learning”, 1st Edition, McGraw Hill Education, 2017.
3. Abhishek Kumar, K. Srinivasa Rao , Suman Lata Tripathi (Editor), “Machine Learning Techniques for VLSI Chip Design Hardcover — Import, 16 July 2023.
4. Abhishek Kumar, Suman Lata Tripathi, K. Srinivasa Rao, “Machine Learning for VLSI Chip Design”, First published:14 July 2023, Print ISBN:9781119910398 |Online ISBN:9781119910497 |DOI:10.1002/9781119910497 , 2023 Scrivener Publishing LLC

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Course Contents and Lecture Schedule		
S. No.	**Topics**	**No. of hours**
1.0	**Machine Learning –Pre-processing to Performance**	
1.1	Machine Learning - Types - Pre-processing	1
1.2	Feature engineering	1
1.3	Feature transformation	1
1.4	Feature Subset Selection	1
1.5	Feature embedding - Training a mode	1
1.6	Preparing to model - Data	1
1.7	Modelling and evaluation	1
1.8	Evaluating performance of a model	1
1.9	Improving performance.	1
2.0	Supervised Learning	
2.1	Linear regression	1
2.2	Logistic regression	1
2.3	Decision Tree	1
2.4	Rule-based classification	1
2.5	Support vector machines	1
2.6	Radial basis functions	1
2.7	Neural and belief networks	1
2.8	Perceptron - Multi-layer feed forward network	1
2.9	Naïve Bayes classifier	1
3.0	**Unsupervised Learning and Ensemble Methods**	
3.1	K-means clustering	1
3.2	Hierarchical methods – Fuzzy clustering	1
3.3	Principal component analysis (PCA) - Linear Discriminant Analysis (LDA),	1
3.4	Partitioning methods	1
3.5	Density based methods DBSCAN - Finding patterns using association rules	1
3.6	Finding patterns using association rules	1
3.7	Markov Chain Monte Carlo Methods	1
3.8	Hidden Markov Model	1
3.9	Bagging and Boosting	1
4.0	**Machine Learning - VLSI Test and Verification**	
4.1	VLSI Testing Process	1
4.2	Off-Chip Testing	1

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

4.3	On-Chip Testing	1
4.4	Combinational Circuit Testing	1
4.5	Sequential Circuit Testing	1
4.6	ML Advantages-Verification Process	1
4.7	Time-Saving	1
4.8	3Ps (Power, Performance, Price)	1
4.9	Electronic Design Automation (EDA)	1
5.0	**Applications of ML**	
5.1	ML in manufacturing process	1
5.2	Reducing maintenance costs and improving reliability	1
5.3	Enhancing new design	1
5.4	Mask synthesis	1
5.5	ML in VLSI functional Verification	1
5.6	ML in Physical Design	1
5.7	Floor planning and Placement Optimization	1
5.8	Routing Optimization	1
5.9	Case studies - Power estimation using random forest.	1

Course Designer(s)

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Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

70 PVL E15	VLSI Technology	Category	L	T	P	Credit
		PE	3	0	0	3

Objectives

- Understanding Semiconductor Fabrication Techniques
- Application of Lithography and Mask Generation Methods
- Comparison of NMOS and CMOS Fabrication Technologies
- Analysis of Advanced Processing Techniques in ULSI Circuits
- Utilization of Process Simulation Tools for VLSI Fabrication

Pre-requisites

Nil

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Understanding of semiconductor fabrication techniques	Understand
CO2	Apply lithography and mask generation techniques	Understand
CO3	Compare NMOS and CMOS fabrication technologies	Analyse
CO4	Analyze advanced processing techniques in ULSI circuits	Apply
CO5	Utilize process simulation tools for VLSI fabrication	Apply

Mapping with Programme Outcomes

COs	POs					
	1	2	3	4	5	6
CO1	3	3	-	-	-	-
CO2	3	3	-	2	-	-
CO3	3	3	3	-	-	-
CO4	-	3	3	3	-	-
CO5	-	3	3	3	3	-
3 - Strong; 2 - Medium; 1 - Some						

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	30	15	30
Understand	30	10	20
Apply	-	20	30
Analyse	-	15	20
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

Syllabus

K.S.Rangasamy College of Technology – Autonomous R2025

M.E-VLSI Design

70 PVL E15- VLSI Technology

Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
I	3	0	0	45	3	40	60	100

Processes in Fabrication Oxidation, Diffusion, Ion Implantation, Etching and Deposition, techniques, Characterization of Processes.	[9]
Lithography and Mask generation techniques Advanced Unit-Processors for ULSI Circuit Technologies., Use of RTP, Plasma processes in the fabrication in the fabrication of circuits., Basic Bipolar process Technologies., NMOS Technology	[9]
Mask Sequence Based Fabrication Process for NMOS Transistors Silicon Gate and Metal Gate Technologies. Limitations of NMOS Technology.	[9]
CMOS Technology Process Sequence for CMOS Technology, Advanced CMOS Processes, Design Rule for NMOS and CMOS Technologies as "Constraint" for Layouts	[9]
Process Simulation Use of SUPREM-IV and STEP Simulators for process Design, - Some Examples of actual technologies.	[9]
Total Hours	**45**

Text Book(s):

1. Jan M. Rabaey, Anantha Chandrakasan, and Borivoje Nikolic, "Digital Integrated Circuits: A Design Perspective", Pearson, 2003.
2. Neil H.E. Weste and David Harris, "CMOS VLSI Design: A Circuits and Systems Perspective", Pearson, 2010.

Reference(s):

1. R.J. Baker, "CMOS: Circuit Design, Layout, and Simulation", Wiley-IEEE Press, 2019.
2. Wayne Wolf, "Modern VLSI Design: System-on-Chip Design", Pearson, 2008.
3. S.M. Sze and Kwok K. Ng, "Physics of Semiconductor Devices", Wiley, 2006.
4. John P. Uyemura, "Introduction to VLSI Circuits and Systems", Wiley, 2001.

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Course Contents and Lecture Schedule

S. No.	Topics	No. of hours
1.0	**Processes in Fabrication**	
1.1	Oxidation	2
1.2	Diffusion	2
1.3	Ion Implantation	2
1.4	Etching and Deposition techniques	2
1.5	Characterization of Processes	1
2.0	**Lithography and Mask generation techniques**	
2.1	Advanced Unit-Processors for ULSI Circuit Technologies	2
2.2	Use of RTP	2
2.3	Plasma processes in the fabrication in the fabrication of circuits	2
2.4	Basic Bipolar process Technologies	1
2.5	NMOS Technology	2
3.0	**Mask Sequence Based Fabrication Process for NMOS Transistors**	
3.1	Silicon Gate and Metal Gate Technologies	4
3.2	Limitations of NMOS Technology	5
4.0	**CMOS Technology**	
4.1	Process Sequence for CMOS Technology	3
4.2	Advanced CMOS Processes	2
4.3	Design	2
4.4	Rule for NMOS and CMOS Technologies as “Constraint” for Layouts	2
5.0	**Process Simulation**	
5.1	Use of SUPREM-IV ans STEP Simulators for process Design	4
5.2	Some Examples of actual technologies.	5

Course Designer(s)

Mr.S.Saravanan- saravanan.s@ksrct.ac.in

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

70 PAC 001	English for Research Paper Writing	Category	L	T	P	Credit
		AC	2	0	0	0

Objectives

- Teach how to improve writing skills and level of readability
- Tell about what to write in each section
- Summarize the skills needed when writing a Title
- Infer the skills needed when writing the Conclusion
- Ensure the quality of paper at very first-time submission

Pre-requisites

- Nil

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Understand that how to improve your writing skills and level of readability	Understand
CO2	Learn about what to write in each section	Understand
CO3	Understand the skills needed when writing a Title	Understand
CO4	Understand the skills needed when writing the Conclusion	Understand
CO5	Ensure the good quality of paper at very first-time submission	Apply

Mapping with Programme Outcomes

COs	POs					
	1	2	3	4	5	6
CO1	3	3	2	3	3	3
CO2	3	3	2	3	3	3
CO3	3	3	2	3	3	3
CO4	3	3	2	3	3	3
CO5	3	3	2	3	3	3
3 - Strong; 2 - Medium; 1 - Some						

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)	
	1	2
Remember	50	40
Understand	50	50
Apply	-	10
Analyse	-	-
Evaluate	-	-
Create	-	-
Total	100	100

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Syllabus

K.S.Rangasamy College of Technology – Autonomous R2025								
Common to all Branches								
70 PAC 001 – English for Research Paper Writing								
Semester	**Hours/Week**			**Total Hours**	**Credit**	**Maximum Marks**		
	L	T	P		C	CA	ES	Total
I	2	0	0	30	0	100	-	100

Introduction to Research Paper Writing Planning and Preparation, Word Order, Breaking up Long Sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness.	[6]
Presentation Skills Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticizing, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts, Introduction.	[6]
Title Writing Skills Key Skills are needed when Writing a Title, Key Skills are Needed when Writing an Abstract, Key Skills are Needed when Writing an Introduction, skills needed when Writing a Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check.	[6]
Result Writing Skills Skills are Needed when Writing the Methods, Skills Needed when Writing the Results, Skills are needed when Writing the Discussion,Skills are Needed when Writing the Conclusions.	[6]
Verification Skills Useful phrases, Checking Plagiarism, how to Ensure paper is as Good as it could Possibly be the First Time Submission.	[6]
Total Hours	**30**

Text book(s):	
1	Adrian Wallwork, English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011.
2	Day R How to Write and Publish a Scientific Paper, Cambridge University Press 2006.
Reference(s):	
1.	Goldbort R Writing for Science, Yale University Press (available on Google Books) 2006.
2.	Highman N, Handbook of Writing for the Mathematical Sciences, SIAM. Highman's book 1998.
3.	Phill Williams, Advanced Writing skills for students of English, Rumian Publishers, 2018.
4.	Sudhir S. Pandhye, English Grammar and Writing Skills, Notion Press, 2017.

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

70 PVL 1P1	VLSI Laboratory I	Category	L	T	P	Credit
		PC	0	0	4	2

Objectives

- To apply Verilog HDL to design and simulate combinational and sequential digital circuits
- To develop parameterized and reusable hardware modules including FSMs and IP cores.
- To analyze and optimize arithmetic subsystems such as adders and multipliers for performance and power efficiency
- To implement pipelined and application-specific digital systems on FPGA platforms
- To interface FPGA with sensors and peripherals to build real-time embedded applications like smart home and health monitoring systems.

Pre-requisites

- Courses on Digital System design and Verilog HDL at UG Level

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Design, simulate, and verify digital circuits using Verilog HDL with waveform and testbench analysis.	Apply
CO2	Implement parameterized FSMs and custom IP cores for modular hardware design.	Apply
CO3	Analyze and synthesize optimized arithmetic circuits for low power and high performance.	Apply
CO4	Deploy pipelined and application-specific digital systems on FPGA using suitable design tools.	Apply
CO5	Integrate FPGA-based designs with sensors and implement real-time systems in domains like healthcare, automation, and image processing.	Apply

Mapping with Programme Outcomes

Cos	POs					
	1	2	3	4	5	6
CO1	3	3	3	2	2	3
CO2	3	3	3	2	2	3
CO3	3	3	3	2	2	3
CO4	3	3	3	2	2	3
CO5	3	3	3	2	2	3
3 - Strong; 2 - Medium; 1 - Some						

Assessment Pattern

Bloom's Category	Lab Experiments Assessment (Marks)		Model Examination (Marks)	End Sem Examination (Marks)
	Lab	Activity		
Remember	-	-	-	-
Understand	-	-	20	20
Apply	50	25	80	80
Analyse	-	-	-	-
Evaluate	-	-	-	-
Create	-	-	-	-
Total	50	25	100	100

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Syllabus

K.S.Rangasamy College of Technology – Autonomous R2025								
M.E-VLSI Design								
70 PVL 1P1 – VLSI Laboratory I								
Semester	**Hours/Week**			**Total Hours**	**Credit**	**Maximum Marks**		
	L	T	P		C	CA	ES	Total
I	0	0	4	60	2	60	40	100

List of Experiments

1. Design and Simulation of Basic Combinational Circuits using Verilog HDL and test benches and waveform analysis
2. Design and Simulation of Sequential Circuits using Verilog HDL and test benches and waveform analysis
3. Design and Implementation of parameterized Finite State Machines (FSM) in Verilog HDL
4. Design and Analysis of Low Power, High-Speed Adders using Verilog HDL
5. Design and Implementation of Optimized Multiplier Architectures
6. Implementation of Arithmetic Logic Unit (ALU) with pipelining on FPGA
7. FPGA-based Implementation of Face/Object Detection Algorithm for Image Processing
8. Design and Deployment of Smart Home Control System using FPGA
9. Implementation of Health Monitoring System using FPGA and Sensors
10. Design and Synthesis of Parameterized IP Cores in Verilog HDL

Course Designer(s)

Dr.D.Mugilan - mugilan@ksrct.ac.in

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

70 PVL 1P2	Analog IC Design Laboratory	Category	L	T	P	Credit
		PC	0	0	4	2

Objectives

- To carry out a detailed analog circuit design starting with transistor characterization and finally realizing an IA design.
- To apply various stages of design, exposure to state of art CAD VLSI tool in various phases of experiments designed
- To bring out the key aspects of each important module in the CAD tool including the simulation
- To design differential amplifier and analyze the performance
- To design layout, LVS and parasitic extracted simulation using CAD tools

Pre-requisites

- Courses on Semiconductor Devices and Circuits and Linear IC Applications at UG Level

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Design digital and analog circuit using CMOS given a design specification.	Analyse
CO2	Design and carry out time domain and frequency domain simulations of simple analog building blocks, study the pole zero behaviors and compute the input/output impedances	Analyse
CO3	Develop layout for the CMOS circuit	Analyse
CO4	Analyze the performance of different amplifiers	Analyse
CO5	Use EDA tools for Circuit Design	Analyse

Mapping with Programme Outcomes

COs	POs					
	1	2	3	4	5	6
CO1	3	3	3	3	2	3
CO2	3	3	3	3	2	3
CO3	3	3	3	3	2	3
CO4	3	3	3	3	2	3
CO5	3	3	3	3	2	3
3 - Strong; 2 - Medium; 1 - Some						

Assessment Pattern

Bloom's Category	Lab Experiments Assessment (Marks)		Model Examination (Marks)	End Sem Examination (Marks)
	Lab	Activity		
Remember	-	-	-	-
Understand	-	-	20	20
Apply	50	25	80	80
Analyse	-	-	-	-
Evaluate	-	-	-	-
Create	-	-	-	-
Total	50	25	100	100

Syllabus

K.S.Rangasamy College of Technology – Autonomous R2025

M.E-VLSI Design

70 PVL 1P2 - Analog IC Design Laboratory

Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
I	0	0	4	60	2	60	40	100

List of Experiments:

CYCLE-I

1. Extraction of process parameters of CMOS process transistors
   a. Plot ID vs. VGS at different drain voltages for NMOS, PMOS.
   b. Plot ID vs. VGS at particular drain voltage for NMOS, PMOS and determine Vt.
   c. Plot log ID vs. VGS at particular gate voltage for NMOS, PMOS and determine IOFF and sub- threshold slope.
   d. Plot ID vs. VDS at different gate voltages for NMOS, PMOS and determine Channel length modulation factor.
   e. Extract Vth of NMOS/PMOS transistors (short channel and long channel). Use VDS of appropriate voltage To extract Vth use the following procedure.
      a. Plot gm vs VGS using SPICE and obtain peak gm point.
      b. Plot y= ID/(gm) as a function of VGS using SPICE.
      c. Use SPICE to plot tangent line passing through peak gm point in y (VGS) plane and determine Vth.
   f. Plot Io vs. Vos at different drain voltages for NMOS, PMOS, plot DC load line and calculate gm, gds, gm/gds, and unity gain frequency. Tabulate result according to technologies and comment on it.
2. CMOS inverter design and performance analysis
   a. i. Plot VTC curve for CMOS inverter and thereon plot dVout vs. dVin, and determine transition voltage and gain g. Calculate VIL, VIH, NMH, NML for the inverter.
      ii. Plot VTC for CMOS inverter with varying VDD.
      iii. Plot VTC for CMOS inverter with varying device ratio.

   b. Perform transient analysis of CMOS inverter with no load and with load and determine propagation delay tpHL, tpLH, 20%-to-80% rise time tr and 80%-to-20% fall time tf.

   c. Perform AC analysis of CMOS inverter with fanout 0 and fanout 1.

3. Use spice to build a three stage and five stage ring oscillator circuit and compare its frequencies.

4. Use FFT and verify the amplitude and frequency components in the spectrum.

CYCLE-II

4. Single stage amplifier design and performance analysis
   a. Plot small signal voltage gain of the minimum-size inverter in the technology chosen as a function of input DC voltage. Determine the small signal voltage gain at the switching point using spice and compare the values for two different process transistors.
   b. Consider a simple CS amplifier with active load, with NMOS transistor as driver and PMOS transistor as load.
      i. Establish a test bench to achieve VDSQ=VDD/2.

i) Determine small signal voltage gain, -3dB BW and GBW of the amplifier
ii) using small signal analysis in spice, considering load capacitance.
iii) Plot step response of the amplifier with a specific input pulse amplitude.
iv) Derive time constant of the output and compare it with the time constant resulted from -3dB Band Width.
v) Use spice to determine input voltage range of the amplifier
vi) Calculate input bias voltage for a given bias current.
vii) Use spice and obtain the bias current. Compare with the theoretical value

5. Three OPAMP Instrumentation Amplifier (INA).
Use proper values of resistors to get a three OPAMP INA with differential-mode voltage gain=10. Consider voltage gain=2 for the first stage and voltage gain=5 for the second stage.
i. Draw the schematic of op-amp macro model.
ii. Draw the schematic of INA.
iii. Obtain parameters of the op-amp macro model such that it meets a given specification for:
i. low-frequency voltage gain,
ii. unity gain BW (fu),
iii. input capacitance,
iv. output resistance,
v. CMRR
iv. Draw schematic diagram of CMRR simulation setup.
v. Simulate CMRR of INA using AC analysis (it's expected to be around 6dB below CMRR of OPAMP).
vi. Plot CMRR of the INA versus resistor mismatches (for resistors of second stage only) changing from -5% to +5% (use AC analysis). Generate a separate plot for mismatch in each resistor pair. Explain how CMRR of OPAMP changes with resistor mismatches.
vii. Repeat (iii) to (vi) by considering CMRR of all OPAMPs with another low frequency gain setting.

6. Use Layout editor.
a. Draw layout of a minimum size inverter using transistors from CMOS process library. Use Metal-1 as interconnect line between inverters.
b. Run DRC, LVS and RC extraction. Make sure there is no DRC error.
c. Extract the netlist. Use extracted netlist and obtain tpHL, tpLH for the inverter using Spice.
d. Use a specific interconnect length and connect and connect three inverters in a chain.
e. Extract the new netlist and obtain teat and tee of the middle inverter.
f. Compare new values of delay times with corresponding values obtained in part 'c'.

7. Design a differential amplifier with resistive load using transistors from CMOS process library that meets a given specification for the following parameter
a. low-frequency voltage gain,
b. unity gain BW (fu),
c. Power dissipation
i. Perform DC analysis and determine input common mode range and compare with the theoretical values.
ii. Perform time domain simulation and verify low frequency gain.
iii. Perform AC analysis and verify.

Course Designer(s)

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Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

K.S. RANGASAMY COLLEGE OF TECHNOLOGY, TIRUCHENGODE - 637215
(An Autonomous Institution affiliated to Anna University)

M.E. / M.Tech. Degree Programme

SCHEME OF EXAMINATIONS
(For the candidates admitted in 2025-2026)

SECOND SEMESTER

S.No.	Course Code	Name of the Course	Duration of Internal Exam	Weightage of Marks			Minimum Marks for Pass in End Semester Exam	
				Continuous Assessment *	End Semester Exam **	Max. Marks	End Semester Exam	Total
THEORY								
1.	70 PVL 201	Solid State Device Modelling	2	40	60	100	45	100
2.	70 PVL 202	VLSI Design Automation	2	40	60	100	45	100
3.	70 PVL 203	VLSI Testing	2	40	60	100	45	100
4.	70 PVL 204	ASIC Design	2	40	60	100	45	100
5.	70 PVL E3*	Professional Elective II	2	40	60	100	45	100
6.	70 PVL E4*	Professional Elective III	2	40	60	100	45	100
7.	70 PAC 002	Disaster Management	2	100	-	100	-	100
PRACTICAL								
8.	70 PVL 2P1	VLSI Laboratory II	3	60	40	100	45	100
9.	70 PVL 2P2	Term Paper and Seminar	3	100	00	100	-	100

* CA evaluation pattern will differ from course to course and for different tests. This will have to be declared in advance to students. The department will put a process in place to ensure that the actual test paper follow the declared pattern.

** End semester Examination will be conducted for maximum marks of 100 and subsequently be reduced to 60 marks for theory End Semester Examination and 40 marks for practical End semester Examination.

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

70 PVL 201	Solid State device Modelling and Simulation	Category	L	T	P	Credit
		PC	3	0	0	3

Objectives

- To apply the knowledge of device physics in modeling of integrated diode.
- To analyze and model MOS capacitor.
- To analyze and model MOSFET, FINFET and UTB.
- To analyze and model MESFET, HBT, HEMT MODFET
- To analyze and model Optoelectronic Devices

Pre-requisites

- Semiconductor devices and Circuits

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Acquire the knowledge of modelling of integrated diode	Understand
CO2	Model and simulate MOS capacitor for different values of process and operating parameters	Apply
CO3	Model and simulate SPICE, EKV and BSIM model of MOSFETs	Analyse
CO4	Acquire the knowledge of modelling SoI, multigate MOSFET, UTB and FINFET devices	Apply
CO5	Acquire the knowledge of modelling of Optoelectronic devices	Apply

Mapping with Programme Outcomes

COs	POs					
	1	2	3	4	5	6
CO1	3	3	-	-	2	3
CO2	3	3	3	3	2	3
CO3	3	3	-	3	2	3
CO4	3	3	-	-	2	3
CO5	3	3	3	3	2	3
3 - Strong; 2 - Medium; 1 - Some						

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	14	6	10
Understand	14	6	10
Apply	32	38	70
Analyse	-	10	10
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Chairman
BoS / ECE
CHAIRMAN BOARD OF STUDIES
Department of ECE
K.S.Rangasamy College of Technology
Tiruchengode - 637 215.

Syllabus

K.S.Rangasamy College of Technology – Autonomous R2025

M.E-VLSI Design

70 PVL 201 - Solid State Device Modelling and Simulation

Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
II	3	0	0	45	3	40	60	100

Introduction to Semiconductor Physics and Diode Modelling Review of Quantum Mechanics - Boltzman transport equation - Continuity equation - Poisson equation. Junction and Schottky diodes in monolithic technologies - static and dynamic behavior - small and large signal models, SPICE modeling and simulation of PN junction and Schottky diode.	[9]
Integrated MOS Capacitance Band diagram- flat band condition and flat band voltage-surface accumulation, surface depletion threshold condition and threshold voltage, charge versus gate voltage, MOS C-V Characteristics, Poly Si gate depletion-effective Increase in Tox.	[9]
Integrated MOS Transistor NMOS and PMOS Transistor - Threshold voltage - Threshold voltage equations - MOS device equations - Basic DC equations Second order effects - Small signal AC Characteristics- MOS models SPICE model, EKV Model, BSIM Model. Technology scaling for cost, speed and power consumption, Subthreshold Current –Subthreshold Swing, Threshold voltage Roll Off-Short Channel Leakage, reducing gate insulator electrical thickness And Tunneling Leakage, Short Channel Effects. Ultra Thin body, SOI and Multigate MOSFET - FINFET. Compact Model for Circuit Simulation using Verilog A	[9]
Advanced Semiconductor Devices MESFETs, HBTs, HEMTs, MOSFETs.	[9]
Optoelectronics Devices Light Emitting Diodes, Lasers, Photoconductors, Junction Photodiodes, Avalanche Photodiodes, Solar Cells	[9]
Total Hours	**45**

Text Book(s):

1. Tyagi M S, "Introduction to Semi-conductor Materials and Devices", John Wiley, 2008
2. S. A. Neamen and D. Biswas, Semiconductor Physics and Devices, 4th Edition, TMH, 2012

Reference(s):

1. P. Bhattacharya, Semiconductor Optoelectronics Devices, 2nd Edition, PHI, 2019.

*SDG 4: Quality education.

**SDG 9: Promote inclusive and sustainable industrialization.

Passed in BoS Meeting held on 13/06/2025

Approved in Academic Council Meeting held on 19/07/2025

Course Contents and Lecture Schedule

S. No.	Topics	No. of hours
1.0	**Introduction to Semiconductor Physics and Diode Modelling**	
1.1	Review of Quantum Mechanics	1
1.2	Boltzman transport equation	1
1.3	Continuity equation	1
1.4	Poisson equation	1
1.5	Junction and Schottky diodes in monolithic technologies	2
1.6	static and dynamic behavior	1
1.7	small and large signal models	1
1.8	SPICE modeling and simulation of PN junction and Schottky diode	1
2.0	**Integrated MOS Capacitance**	
2.1	Band diagram	1
2.2	flat band condition and flat band voltage-surface accumulation	1
2.3	surface depletion	1
2.4	threshold condition and threshold voltage	1
2.5	charge versus gate voltage	1
2.6	MOS C-V Characteristics	1
2.7	Poly Si gate depletion	1
2.9	Effective Increase In Tox	1
3.0	**Integrated MOS Transistor**	
3.1	NMOS and PMOS Transistor	1
3.2	Threshold voltage	1
3.3	Threshold voltage equations	1
3.4	MOS device equations - Basic DC equations Second order effects	1
3.5	Small signal AC Characteristics- MOS models SPICE model	1
3.6	EKV Model, BSIM Model	1
3.7	Technology scaling for cost, speed and power consumption	1
3.8	Subthreshold Current –Subthreshold Swing	1
3.9	Threshold voltage Roll Off-Short Channel Leakage	1
3.10	reducing gate insulator electrical thickness And Tunneling Leakage, Short Channel Effects. Ultra Thin body	1
3.11	SOI and Multigate MOSFET - FINFET. Compact Model for Circuit Simulation using Verilog A	1
4.0	**Advanced Semiconductor Devices**	
4.1	MESFETs	2
4.2	HBTs	2
4.3	HEMTs	2
4.4	MOSFETs	2
5.0	**Optoelectronics Devices**	
5.1	Light Emitting Diodes	2
5.2	Lasers	1
5.3	Photoconductors	2

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5.4	Junction Photodiodes	2
5.5	Avalanche Photodiodes	1
5.6	Solar Cells	1

Course Designer(s)

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Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

70 PVL 202	VLSI Design Automation	Category	L	T	P	Credit
		PC	3	0	0	3

Objectives

- To acquire the knowledge in Design methodologies.
- To familiarize in the basic concepts of Layout
- To acquire the knowledge in various modeling
- To get exposed in the hardware model
- To get exposed in FPGA Technologies

Pre-requisites

- Analog and Digital CMOSVLSI design

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Apply the graph and partitioning algorithms on addressing Computational complexity	Apply
CO2	Apply the floor planning and placement routing algorithms	Apply
CO3	Analyze modeling of various Designs	Analyse
CO4	Understand hardware models and scheduling	Apply
CO5	Interpret and analyze FPGA technologies and Apply the routing Algorithms for high-level transformation	Analyse

Mapping with Programme Outcomes

COs	POs					
	1	2	3	4	5	6
CO1	3	3	3	2	3	3
CO2	3	3	2	2	3	3
CO3	3	3	3	2	2	2
CO4	3	3	3	3	2	2
CO5	3	3	2	3	3	3
3 - Strong; 2 - Medium; 1 - Some						

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	20	15	30
Understand	30	10	20
Apply	10	20	30
Analyse	-	15	20
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

K.S. Rangasamy College of Technology – Autonomous R 2025								
M.E-VLSI Design								
70 PVL 202 – VLSI Design Automation								
Semester	Hours / Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
II	3	0	0	45	3	40	60	100

Introduction to Design Methodologies* Design Automation tools, Algorithmic Graph Theory, Computational Complexity, Tractable and Intractable Problems	[9]
Layout* Compaction, Placement, Floor planning and Routing Problems, Concepts and Algorithms	[9]
Modeling* Gate Level Modeling and Simulation, Switch level modeling and simulation, Basic issues and Terminology, Binary — Decision diagram, Two — Level Logic Synthesis	[9]
Hardware Models* Internal representation of the input algorithm, Allocation, Assignment and Scheduling, Some Scheduling Algorithms, Some aspects of Assignment problem, High — level Transformations.	[9]
FPGA technologies** Physical Design cycle for FPGA's partitioning and routing for segmented and staggered models. MCM technologies, MCM physical design cycle, Partitioning, Placement — Chip array based and full custom approaches, Routing –Maze routing, Multiple stage routing, Topologic routing, Integrated Pin — Distribution and routing, routing and programmable MCM's.	[9]
Total Hours	**45**

Text Book(s):	
1.	S.H.Gerez, "Algorithms for VLSI Design Automation", John Wiley 1999.
2.	Naveed Sherwani, "Algorithms for VLSI Physical Design Automation", 3rd Edition, Springer International Edition.
Reference(s):	
1.	Hill & Peterson, "Computer Aided Logical Design with Emphasis on VLSI", Wiley,1993
2.	Wayne Wolf, "Modern VLSI Design: Systems on silicon", 2nd Edition, Pearson Education Asia.

*SDG: 4- Quality Education

**SDG: 8 – Decent work and Economic growth

Passed in BoS Meeting held on 13/06/2025

Approved in Academic Council Meeting held on 19/07/2025

Course Contents and Lecture Schedule

S.No	Topic	No. of Hours
1	**Introduction to Design Methodologies**	
1.1	Design Automation tools	1
1.2	Data structure for the representation of Graphs	1
1.3	Computational complexity	1
1.4	Examples of graph algorithms	2
1.5	Combinational optimization problems	1
1.6	Decision problems	1
1.7	Complexity classes & Consequences	1
1.8	NP-Completeness and NP-hardness	1
2	**Layout**	
2.1	Layout Compaction: Design rules & symbolic layout	1
2.2	Algorithms for Constrained graph compaction	1
2.3	Placement: Circuit representation & Wire length Estimation	1
2.4	Placement algorithms	1
2.5	Floor planning	2
2.6	Routing Problems: Area routing & channel routing	1
2.7	Introduction to global routing and Algorithms for global routing	2
3	**Modeling**	
3.1	Gate Level Modeling and Simulation: Signal, Gate modeling & Delay modeling	1
3.2	Connectivity modeling, Compiler & event driven simulation	1
3.3	Switch level modeling and simulation: Connectivity and signal modeling	1
3.4	Simulation mechanisms	1
3.5	Basic issues and Terminology	1
3.6	Binary – Decision diagram	2
3.7	Two – Level Logic Synthesis: Problem definition and analysis	1
3.8	A Heuristic based in ROBDDs	1
4	**Hardware Models**	
4.1	Internal representation of the input algorithm	2
4.2	Allocation, Assignment and Scheduling	2
4.3	Some Scheduling Algorithms	2
4.4	Some aspects of Assignment problem	2
4.5	High – level Transformations	1
5	**FPGA Technologies**	
5.1	Physical Design cycle for FPGA's partitioning	1
5.2	Routing for segmented and staggered models	1
5.3	MCM technologies, MCM physical design cycle	1
5.5	Partitioning, Placement – Chip array based and full custom approaches	1
5.6	Routing –Maze routing	1
5.7	Multiple stage routing	1

5.8	Topologic routing	1
5.9	Integrated Pin – Distribution and routing, routing and programmable MCM's	1

Course Designers

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Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

70 PVL 203	VLSI Testing	Category	L	T	P	Credit
		PC	3	0	0	3

Objectives

- To introduce the VLSI testing
- To introduce the logic and fault simulation and testability measures
- To study the test generation for combinational and sequential circuits
- To study the design for testability
- To study the fault diagnosis

Pre-requisites

- Analog and Digital CMOS VLSI design

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Understand the basics of VLSI testing	Remember
CO2	Discuss logic simulation techniques and perform fault simulation to detect potential faults in VLSI designs	Understand
CO3	Evaluate testability measures and apply Design for Testability (DFT) principles to enhance fault detection in digital systems.	Analyse
CO4	Examine floor-planning techniques, including block placement, routing, and clock distribution for optimized VLSI design.	Analyse
CO5	Analyze the techniques used for fault diagnosis in VLSI systems and apply fault detection methods for enhanced system reliability.	Analyse

Mapping with Programme Outcomes

COs	POs					
	1	2	3	4	5	6
CO1	3	3	2	3	3	3
CO2	3	3	3	2	3	3
CO3	3	2	3	3	3	3
CO4	3	3	3	3	2	3
CO5	3	3	3	3	3	3
3 - Strong; 2 - Medium; 1 - Some						

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	30	20	30
Understand	30	10	20
Apply	-	20	20
Analyse	-	10	30
Evaluate	-	-	
Create	-	-	
Total	60	60	100

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Syllabus

K.S.Rangasamy College of Technology – Autonomous R2025								
M.E-VLSI Design								
70 PVL 203-VLSI Testing								
Semester	**Hours/Week**			**Total Hours**	**Credit**	**Maximum Marks**		
	L	T	P		C	CA	ES	Total
II	3	0	0	45	3	40	60	100

Introduction to Test Introduction, VLSI Testing Process and Test Equipment, Challenges in VLSI Testing, Test Economics and Product Quality, Fault Modeling, Relationship Among Fault Models.	[9]
Logic & Fault Simulation & Testability Measures Simulation for Design Verification and Test Evaluation, Modeling Circuits for Simulation, Algorithms for True Value and Fault Simulation, Scoap Controllability and Observability	[9]
Test Generation for Combinational and Sequential Circuits* Introduction to Test Generation-Overview of Testing in Digital Circuits, Fault Models for Combinational Circuits, Test Generation for Combinational Circuits, Introduction to Sequential Circuits, Test Generation for Sequential Circuits, Applications of Test Generation Techniques	[9]
Design for Testability Design for Testability Basics, Testability Analysis, Scan Cell Designs, Scan Architecture, Built in Self-Test, Random Logic BIST, DFT for Other Test Objectives	[9]
Fault Diagnosis Introduction and Basic Definitions, Fault Models for Diagnosis, Generation of Vectors for Diagnosis, Combinational Logic Diagnosis, Scan Chain Diagnosis, Logic BIST Diagnosis.	[9]
Total Hours	45

Text Book(s):

1. Michael L. Bushnell and Vishwani D. Agrawal “Essentials of Electronic Testing for Digital, Memory, and Mixed-Signal VLSI Circuits”,2020
2. Niraj K Jha and Sandeep Gupta “Testing of Digital Systems”,2023

References:

1. Laung-Terng Wang, Cheng-Wen Wu and Xiaoqing Wen, “VLSI Test Principles and Architectures”, Elsevier, 2017
2. Michael L. Bushnell and Vishwani D. Agrawal, “Essentials of Electronic Testing for Digital, Memory & Mixed-Signal VLSI Circuits” Kluwer Academic Publishers, 2017.
3. Niraj K. Jha and Sandeep Gupta, “Testing of Digital Systems”, Cambridge University Press, 2017.

* SDG 9 – Industry, Innovation, and Infrastructure

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Course Contents and Lecture Schedule

S. No.	Topics	No. of hours
1	**Introduction to Testing**	
1.1	Introduction to VLSI Testing	2
1.2	VLSI Testing Process and Test Equipment	2
1.3	Challenges in VLSI Testing	1
1.4	Test Economics and Product Quality	1
1.5	Fault Modelling	2
1.6	Relationship Among Fault Models	1
2	**Logic & Fault Simulation & Testability Measures**	
2.1	Simulation for Design Verification and Test Evaluation	2
2.2	Modelling Circuits for Simulation	2
2.3	Algorithms for True Value Simulation	2
2.4	Algorithms for Fault Simulation	2
2.5	Scoap Controllability and Observability	1
3	**Test Generation for Combinational and Sequential Circuits**	
3.1	Introduction to Test Generation	1
3.2	Overview of Testing in Digital Circuits	1
3.3	Fault Models for Combinational Circuits	2
3.4	Test Generation for Combinational Circuits	2
3.5	Introduction to Sequential Circuits	1
3.6	Test Generation for Sequential Circuits	1
3.7	Applications of Test Generation Techniques	1
4	**Design for Testability**	
4.1	Design for Testability Basics	2
4.2	Testability Analysis	2
4.3	Scan Cell Designs	1
4.4	Scan Architecture	1
4.5	Built-in Self-Test (BIST)	1
4.6	Random Logic BIST	1
4.7	DFT for Other Test Objectives	1
5	**Fault diagnosis**	
5.1	Introduction and Basic Definitions	2
5.2	Fault Models for Diagnosis	2
5.3	Generation of Vectors for Diagnosis	2
5.4	Combinational Logic Diagnosis	1
5.5	Scan Chain Diagnosis	1
5.6	Logic BIST Diagnosis	1

Course Designer(s)

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Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

70 PVL 204	ASIC Design	Category	L	T	P	Credit
		PC	3	0	0	3

Objectives

- To know on the types of ASIC design and ASIC library design
- To introduces the principles of design logic cells, I/O Cells and Interconnect architecture
- To analyze various programmable ASIC architecture with logic cells, I/O Cells and Interconnect architecture
- To analyze high performance algorithms for floor planning and placement and routing of cells in ASIC design
- To deal with the entire FPGA and ASIC design flow from the circuit and layout design point of view

Pre-requisites

- Digital Logic Design

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Apply logical effort technique for predicting delay, delay minimization and FPGA architectures	Apply
CO2	Design logic cells and I/O cells	Apply
CO3	Analyze the various resources of recent FPGAs	Analyse
CO4	Use algorithms for floor planning and placement of cells, routing for optimization of power and speed and understand the concept of layout static time analyses	Apply
CO5	Analyze high performance algorithms available for ASICs	Analyse

Mapping with Programme Outcomes

COs	POs					
	1	2	3	4	5	6
CO1	-	-	-	-	-	3
CO2	-	-	-	2	-	3
CO3	3	2	3	2	3	3
CO4	3	2	3	3	2	3
CO5	2	-	-	3	-	3
3 - Strong; 2 - Medium; 1 - Some						

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	10	10	10
Understand	35	35	60
Apply	15	10	20
Analyse	-	5	10
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Syllabus

K.S.Rangasamy College of Technology – Autonomous R2025

M.E-VLSI Design

70 PVL 204 - ASIC Design

Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
II	3	0	0	45	3	40	60	100

Introduction to ASIC'S, CMOS Logic and ASIC Library Design Types of Asics - Design Flow - Traditional and Physical Compiler based ASIC Flow- CMOS Transistors - Combinational Logic Cell – Sequential Logic Cell - Data Path Logic Cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical Effort.	[9]
Programmable ASIC's, Programmable ASIC Logic Cells and Programmable ASIC I/O Cells Antifuse - Static Ram - EPROM and EEPROM Technology - ACTEL ACT- Xilinx LCA – ALTERA FLEX - ALTERA MAX DC & AC Inputs and Outputs - Clock & Power Inputs - Xilinx I/O Blocks.	[9]
Programmable ASIC Architecture* Architecture and Configuration of ARTIX / Cyclone and KINTEX Ultra Scale / STRATIX FPGA – Micro-Blaze / NIOS Based Embedded Systems – Signal Probing Techniques.	[9]
Logic Synthesis, Static Timing Analysis, Placement and Routing Logic Synthesis, Pre-Layout STA, Floor Planning Goals and Objectives, Floor Planning Tools, I/O Placement and Power Planning, Standard Cell Placement, Clock Tree Synthesis, Timing Optimization, Routing: Global Routing and Detailed Routing, post-layout STA.	[9]
System-on-Chip Design SoC Design Flow, Platform-Based and IP Based SoC Designs, Basic Concepts of Bus-Based Communication Architectures, High Performance Filters using Delta-Sigma Modulators. Case Studies: Digital Camera, SDRAM, High Speed Data standards	[9]
Total Hours	**45**

Text book(s):

1	M.J.S.Smith, "Application Specific Integrated Circuits", Pearson, 2003.
2	Steve Kilts, "Advanced FPGA Design", Wiley Inter-Science,2006.

Reference(s):

1.	Roger Woods, John Mcallister, Dr. Ying Yi, Gaye Lightbod, "FPGA-Based Implementation of Signal Processing Systems", Wiley, 2008.
2.	J.Rabaey, "Low Power Design Essentials (Integrated Circuits and Systems)", Springer, 2009.
3.	David Flynn, Rob Aitken, Alan Gibbons, Kaijian Shi, "Low Power Methodology Manual: For System-on-Chip Design (Integrated Circuits and Systems)" Springer, 2008.
4.	Yuan Taur and Tak H.Ning, "Fundamentals of Modern VLSI Devices", Cambridge University Press, 2016.

*SDG 9: Industry, Innovation, and Infrastructure

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Course Contents and Lecture Schedule

S. No.	Topics	No. of hours
1.0	Introduction **to ASIC'S, CMOS Logic and ASIC Library Design**	
1.1	Types of ASICs	2
1.2	Design Flow - CMOS Transistors	2
1.3	Combinational Logic Cell	1
1.4	Sequential Logic Cell	1
1.5	Data Path Logic Cell	1
1.6	Transistors as Resistors - Transistor Parasitic Capacitance	1
1.7	Logical Effort	1
2.0	**Programmable ASIC's, Programmable ASIC Logic Cells and Programmable ASIC I/O Cells**	
2.1	Antifuse - Static Ram - EPROM and EEPROM Technology	2
2.2	ACTEL ACT	1
2.3	Xilinx LCA	1
2.4	ALTERA FLEX	1
2.5	ALTERA MAX	1
2.6	DC & AC Inputs and Outputs	1
2.7	Clock & Power Inputs	1
2.8	Xilinx I/O Blocks	1
3.0	**Programmable ASIC Architecture**	
3.1	Architecture and Configuration of ARTIX	2
3.2	Cyclone and KINTEX Ultra Scale	2
3.3	STRATIX FPGA	2
3.4	Micro-Blaze / NIOS Based Embedded Systems	2
3.5	Signal Probing Techniques	1
4.0	**Logic Synthesis, Static Timing Analysis, Placement and Routing**	
4.1	Logic Synthesis, Pre-Layout STA	1
4.2	Floor Planning Goals and Objectives, Floor Planning Tools	1
4.3	I/O Placement and Power Planning, Standard Cell Placement	2
4.4	Clock Tree Synthesis, Timing Optimization	2
4.5	Routing: Global Routing and Detailed Routing	1
4.6	Post-Layout STA	2
5.0	**System-on-Chip Design**	
5.1	SoC Design Flow	1
5.2	Platform-Based and IP Based SoC Designs	2
5.3	Basic Concepts of Bus-Based Communication Architectures	1
5.4	High Performance Filters using Delta-Sigma Modulators	2
5.5	Case Studies: Digital Camera, SDRAM, High Speed Data standards.	3

Course Designer(s)

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Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

70 PVL E21	Low Power VLSI Design	Category	L	T	P	Credit
		PE	3	0	0	3

Objectives

- To identify sources of power in an IC
- To identify the power reduction techniques based on technology independent and technology dependent methods
- To identify suitable techniques to reduce the power dissipation
- To estimate power dissipation of various MOS logic circuits
- To develop algorithms for low power dissipation

Pre-requisites

- Analog and Digital CMOS VLSI design

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Understand the power dissipation of MOS circuits	Understand
CO2	Design and analyze various MOS logic circuits	Understand
CO3	Apply low power techniques for low power dissipation	Analyse
CO4	Estimate the power dissipation of ICs	Apply
CO5	Develop algorithms to reduce power dissipation by software	Apply

Mapping with Programme Outcomes

COs	POs					
	1	2	3	4	5	6
CO1	-	-	3	-	-	3
CO2	3	-	3	2	-	3
CO3	-	-	3	-	-	3
CO4	-	-	3	-	-	3
CO5	3	-	3	3	-	3
3 - Strong; 2 - Medium; 1 - Some						

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	30	15	30
Understand	30	10	20
Apply	-	20	30
Analyse	-	15	20
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Syllabus

K.S.Rangasamy College of Technology – Autonomous R2025

M.E-VLSI Design

70 PVL E21 – Low Power VLSI Design

Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
II	3	0	0	45	3	40	60	100

Power Dissipation in CMOS Hierarchy of Limits of Power – Sources of Power Consumption – Physics of Power Dissipation in CMOS FET Devices – Basic Principle of Low Power Design.	[9]
Power Optimization Logic Level Power Optimization – Circuit Level Low Power Design – Gate Level Low Power Design–Architecture Level Low Power Design – VLSI Subsystem Design of Adders, Multipliers, PLL, Low Power Design	[9]
Design of Low Power CMOS Circuits Computer Arithmetic Techniques for Low Power System – Reducing Power Consumption in Combinational Logic, Sequential Logic, Memories – Low Power Clock – Advanced Techniques –Special Techniques, Adiabatic Techniques – Physical Design, Floor Planning, Placement and Routing.	[9]
Power Estimation Power Estimation Techniques, Circuit Level, Gate Level, Architecture Level, Behavioral Level, –Logic Power Estimation – Simulation Power Analysis –Probabilistic Power Analysis	[9]
Synthesis and Software Design for Low Power CMOS Circuits Synthesis for Low Power – Behavioral Level Transform –Algorithms for Low Power – Software Design for Low Power.	[9]
Total Hours	**45**

Text Book(s):

1. Kaushik Roy and S.C.Prasad, “Low Power CMOS VLSI Circuit Design”, Wiley, 2000
2. J.B.Kulo and J.H Lou, “Low Voltage CMOS VLSI Circuits”, Wiley 2019.

Reference(s):

1. James B.Kulo, Shih-Chia Lin, “Low Voltage SOI CMOS VLSI Devices and Circuits”, John Wiley and Sons, Inc. 2001
2. J.Rabaey, “Low Power Design Essentials (Integrated Circuits and Systems)”, Springer, 2009
3. David Flynn, Rob Aitken, Alan Gibbons, Kaijian Shi, “Low Power Methodology Manual: For System-on-Chip Design (Integrated Circuits and Systems)”, Springer, 2008.
4. Yuan Taur and TakH.Ning, "Fundamentals of Modern VLSI Devices", Cambridge University Press, 2016.

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Course Contents and Lecture Schedule

S. No.	Topics	No. of hours
1	**Power Dissipation in CMOS**	
1.1	Hierarchy of Limits of Power	1
1.2	Sources of Power Consumption	2
1.3	Physics of Power Dissipation in CMOS FET Devices	2
1.4	Various power Dissipation	2
1.4	Basic Principle of Low Power Design	2
2	**Power Optimization**	
2.1	Logic Level Power Optimization	1
2.2	Circuit Level Low Power Design	1
2.3	Gate Level Low Power Design	2
2.4	Architecture Level Low Power Design	1
2.5	VLSI Subsystem Design of Adders	1
2.6	Multipliers	1
2.7	PLL	1
2.8	Low Power Design	1
3	**Design of Low Power CMOS Circuits**	
3.1	Computer Arithmetic Techniques for Low Power System	1
3.2	Reducing Power Consumption in Combinational Logic, Sequential Logic, Memories	2
3.3	Low Power Clock	2
3.4	Advanced Techniques	1
3.5	Special Techniques, Adiabatic Techniques	2
3.6	Physical Design, Floor Planning, Placement and Routing	1
4	**Power Estimation**	
4.1	Power Estimation Techniques	1
4.2	Circuit Level, Gate Level	2
4.3	Architecture Level, Behavioral Level	2
4.4	Logic Power Estimation	2
4.5	Simulation Power Analysis	1
4.6	Probabilistic Power Analysis	1
5	**Synthesis and Software Design for Low Power CMOS Circuits**	
5.1	Synthesis for Low Power	2
5.2	Behavioral Level Transform	3
5.3	Algorithms for Low Power	2
5.4	Software Design for Low Power	2

Course Designer(s)

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Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

70 PVL E22	Digital Image Processing	Category	L	T	P	Credit
		PE	3	0	0	3

Objectives

- To understand a fundamental understanding of image concepts and transformations.
- To introduce techniques for image enhancement and restoration.
- To impart comprehensive knowledge of segmentation and recognition methods.
- To develop a thorough understanding of image compression strategies.
- To explore video processing and motion estimation techniques.

Pre-requisites

- Image Processing

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Describe digital image fundamentals and different transforms.	Understand
CO2	Discuss the basics of Image enhancement and restoration techniques of images.	Apply
CO3	Explain the techniques of image segmentation and recognition.	Analyse
CO4	Discuss about color image processing and image compression.	Analyse
CO5	Describe about video processing systems.	Apply

Mapping with Programme Outcomes

COs	POs					
	1	2	3	4	5	6
CO1	3	3	3	2	3	3
CO2	3	3	3	2	3	3
CO3	3	3	3	2	3	3
CO4	3	3	3	2	3	3
CO5	3	3	3	2	3	3
3 - Strong; 2 - Medium; 1 - Some						

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	20	10	30
Understand	20	20	30
Apply	20	20	30
Analyse	-	10	10
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Syllabus

K.S.Rangasamy College of Technology – Autonomous R2025								
M.E-VLSI Design								
70 PVL E22- Digital Image Processing								
Semester	**Hours/Week**			**Total Hours**	**Credit**	**Maximum Marks**		
	L	T	P		C	CA	ES	Total
II	3	0	0	45	3	40	60	100

Digital Image Fundamentals and Transforms Elements of Visual Perception – Image Sampling and Quantization Basic Relationship between Pixels – Basic Geometric Transformations-Introduction to Fourier Transform and DFT – Properties of 2D Fourier Transform – FFT – Separable Image Transforms -Walsh – Hadamard – Discrete Cosine Transform – Haar - Slant – Karhunen Loeve Transforms.	[9]
Image Enhancement and Restoration Basic Gray Level Transformations – Histogram Equalization – Histogram Matching - Spatial Filtering – Smoothing Spatial Filters – Sharpening Spatial Filters- Model of the Image Degradation / Restoration Process- Mean Filters — Order — Statistics Filters- Adaptive Filters – Inverse Filtering – Minimum Mean Square Error Filtering – Constrained Least Squares Filtering – Geometric Mean Filter – Geometric Transformation.	[9]
Image Segmentation and Recognition Detection of Discontinuities – Edge Linking and Boundary Detection – Region Based Segmentation – Morphological Operators: Dilation – Erosion - Opening and Closing - Image Recognition Patterns and Pattern Classes. Recognition Based on Decision – Theoretic Methods.	[9]
Image Compression & Color Image Processing Need for Data Compression, Huffman, Run Length Encoding, Vector Quantization, Transform Coding, JPEG Standard, MPEG. Color Fundamentals – Color Models –Basics of Full-Color Image- Pseudo Color Image Processing Processing-Color Transformations – Smoothing and Sharpening – Image Segmentation Based on Color.	[9]
Basic Steps of Video Processing Analog Video, Digital Video. Time-Varying Image Formation models: Three-dimensional Motion Models, Geometric Image Formation, Photometric Image Formation, Sampling of Video signals, Filtering operations	[9]
Total Hours	**45**

Textbook(s):	
1.	Rafael C Gonzalez, Richard E. Woods, "Digital Image Processing", 4th Edition, Pearson Education, 2018.
2.	Jain A.K., "Fundamentals of Digital Image Processing", New Edition, Prentice Hall of India, 2016.
Reference(s):	
1.	Yao Wang, JoernOstermann, and Ya-Qin Zhang ," Video Processing and Communications", Prentice Hall, 2016.
2.	William K. Pratt, "Digital Image Processing", John Wiley, New York, 2016
3.	Rafael C. Gonzalez Richard E. Woods, Steven Eddins, "Digital Image Processing using MATLAB", Tata Mcgraw Hill, 2016.
4.	J.W. Woods, "Multidimensional Signal, Image, Video Processing and Coding", 2nd Edition, Academic Press, 2016.

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Course Contents and Lecture Schedule		
S. No.	**Topics**	**No. of hours**
1.0	**Digital Image Fundamentals and Transforms**	
1.1	Elements of Visual Perception	1
1.2	Image Sampling and Quantization Basic Relationship between Pixels	1
1.3	Basic Geometric Transformations	1
1.4	Introduction to Fourier Transform and DFT	1
1.5	Properties of 2D Fourier Transform	1
1.6	FFT	1
1.7	Separable Image Transforms, Walsh, Hadamard	1
1.8	Discrete Cosine Transform	1
1.9	Haar – Slant, Karhunen Loeve Transforms.	1
2.0	**Image Enhancement and Restoration**	
2.1	Basic Gray Level Transformations	1
2.2	Histogram Equalization, Histogram Matching	1
2.3	Spatial Filtering, Smoothing Spatial Filters	1
2.4	Sharpening Spatial Filters- Model of the Image Degradation / Restoration Process	1
2.5	Mean Filters – Order – Statistics Filters- Adaptive Filters	1
2.6	Inverse Filtering – Minimum Mean Square Error Filtering	1
2.7	Constrained Least Squares Filtering	1
2.8	Geometric Mean Filter	1
2.9	Geometric Transformations	1
3.0	**Image Segmentation and Recognition**	
3.1	Detection of Discontinuities	1
3.2	Edge Linking and Boundary Detection	1
3.3	Region Based Segmentation	1
3.4	Morphological Operators: Dilation – Erosion	2
3.5	Opening and Closing	1
3.6	Image Recognition Patterns and Pattern Classes	1
3.7	Recognition Based on Decision	1
3.8	Theoretic Methods	1
4.0	**Image Compression& Color Image Processing**	
4.1	Need for Data Compression, Huffman	1
4.2	Run Length Encoding, Vector Quantization	1
4.3	Transform Coding, JPEG Standard, MPEG	1
4.4	Color Fundamentals – Color Models	1
4.5	Basics of Full-Color Image	1
4.6	Processing-Color Transformations	2
4.7	Smoothing and Sharpening	1
4.8	Image Segmentation Based on Color	1
5.0	**Basic Steps of Video Processing**	
5.1	Analog Video, Digital Video	2
5.2	Time-Varying Image Formation models	2
5.3	Three-dimensional Motion Models	2
5.4	Geometric Image Formation	2
5.5	Photometric Image Formation	1

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

5.6	Sampling of Video signals, Filtering operations	1

Course Designer(s)

Dr.S.Malarkhodi - malarkhodi@ksrct.ac.

70 PVL E23	IP Based VLSI Design	Category	L	T	P	Credit
		PE	3	0	0	3

Objectives

- To learn about IC manufacturing and fabrication.
- To analyse the combinational, sequential and subsystem design.
- To analyse the subsystem design.
- To learn about different floor planning techniques and architecture design.
- To introduce IP design security

Pre-requisites

- Digital CMOS VLSI Design

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Describe the IC manufacturing with various fabrication process and Layout design techniques	Understand
CO2	Analyze the combinational logic networks and its functions	Apply
CO3	Design the sequential circuits and analyse the subsystem design performance	Apply
CO4	Describe the various floor planning techniques and architecture in VLSI.	Understand
CO5	Explain an IP based Protection of data and Privacy security.	Understand

Mapping with Programme Outcomes

COs	POs					
	1	2	3	4	5	6
CO1	3	-	3	-	-	3
CO2	3	-	3	3	-	3
CO3	3	-	3	3	-	3
CO4	3	3	3	3	-	3
CO5	3	3	3	-	3	3
3 - Strong; 2 - Medium; 1 - Some						

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	10	10	20
Understand	25	25	40
Apply	25	25	40
Analyse	-	-	-
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Syllabus

K.S.Rangasamy College of Technology – Autonomous R2025								
M.E-VLSI Design								
70 PVL E23- IP Based VLSI Design								
Semester	**Hours/Week**			**Total Hours**	**Credit**	**Maximum Marks**		
	L	T	P		C	CA	ES	Total
II	3	0	0	45	3	40	60	100

VLSI and Its Fabrication Introduction -IC Manufacturing - CMOS Technology - IC Design Techniques - IP Based Design - Fabrication Process-Transistors - Wires and Vias - Fabrication Theory Reliability - Layout Design and Tools.	[9]
Combinational Logic Networks Logic Gates: Combinational Logic Functions - Static Complementary Gates - Switch Logic - Alternate Gate Circuits - Low Power Gates – Delay – Yield - Gates as IP - Combinational Logic Networks-Standard Cell Based Layout- Combinational Network Delay- Logic and Interconnect Design- Power Optimization- Switch Logic Network- Logic Testing.	[9]
Subsystem Design Sequential Machine -Latch and Flip flop - System Design and Clocking - Performance Analysis - Power Optimization - Design Validation and Testing - Subsystem Design- Combinational Shifter- Arithmetic Circuits- High Density Memory - Image Sensors — FPGA – PLA - Buses and NoC - Data paths - Subsystems as IP.	[9]
Floor Planning and Architecture Design Floor Planning -Floor Planning Methods - Global Interconnect - Floor Plan Design - off - Chip Connections Architecture Design - HDL - Register -Transfer Design - Pipelining - High Level Synthesis - Architecture for Low Power - GALS Systems - Architecture Testing - IP Components - Design Methodologies - Multiprocessor System - on-chip Design	[9]
Design Security IP in Reuse Based Design - Constrained Based IP Protection - Protection of Data and Privacy Constrained Based Watermarking for VLSI IP Based Protection	[9]
Total Hours	**45**

Textbook(s):	
1.	Wayne Wolf, “Modern VLSI Design: IP-based Design”, 4th Edition, Prentice Hall of India Private Ltd., 2013.
2.	Qu Gang, Miodrag Potkonjak, “Intellectual Property Protection in VLSI Designs: Theory and Practice”, Springer, 2013.
Reference(s):	
1.	Marilyn Wolf, “Modern Vlsi Design Ip-Based Design”, 4th Edition Prentice Hall of India Private Ltd., 2013.
2.	Swarup Bhunia, Sandip Ray, Susmita Sur-Kolay, "Fundamentals of IP and SoC Security: Design,Verification and Debug", Springer,2017.
3.	Prabhat Mishra, Swarup Bhun, "Mark Tehr ‘Hardware IP Security and Trust”, Springer, 2017.
4.	Charlotte Stedman, “Modern VLSI Design”, Larsen & Keller Education, 2019

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Course Contents and Lecture Schedule		
S. No.	**Topics**	**No. of hours**
1.0	**VLSI and Its Fabrication**	
1.1	Introduction -IC Manufacturing	1
1.2	CMOS Technology	1
1.3	IC Design Techniques	1
1.4	IP Based Design	1
1.5	Fabrication Process	1
1.6	Transistors	1
1.7	Wires and VIAS	1
1.8	Fabrication Theory Reliability	1
1.9	Layout Design and Tools	1
2.0	**Combinational Logic Networks**	
2.1	Logic Gates: Combinational Logic Functions	1
2.2	Static Complementary Gates	1
2.3	Switch Logic - Alternate Gate Circuits	1
2.4	Low Power Gates	1
2.5	Delay, Yield, Gates as IP	1
2.6	Combinational Logic Networks	1
2.7	Standard Cell Based Layout	1
2.8	Combinational Network Delay, Logic and Interconnect Design	1
2.9	Power Optimization, Switch Logic Network, Logic Testing.	1
3.0	**Subsystem Design**	
3.1	Sequential Machine -Latch and Flip flop	1
3.2	System Design and Clocking	1
3.3	Performance Analysis	1
3.4	Power Optimization, Design Validation and Testing	1
3.5	Subsystem Design, Combinational Shifter	1
3.6	Arithmetic Circuits	1
3.7	High Density Memory, Image Sensors	1
3.8	FPGA, PLA	1
3.9	Buses and NoC, Data Paths, Subsystems as IP	1
4.0	**Floor Planning and Architecture Design**	
4.1	Floor Planning, Floor Planning Methods	1
4.2	Global Interconnect, Floor Plan Design	1
4.3	Off -Chip Connections Architecture Design	1
4.4	HDL, Register, Transfer Design	1
4.5	Pipelining, High Level Synthesis	1
4.6	Architecture for Low Power, GALS Systems	1
4.7	Architecture Testing, IP Components	1
4.8	Design Methodologies,	1
4.9	Multiprocessor System, on-Chip Design	1
5.0	**Design Security**	
5.1	IP In Reuse-Based Design	2
5.2	Constrained Based IP Protection	2

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

5.3	Protection of Data and Privacy	2
5.4	Constrained Based Watermarking for VLSI IP Based Protection	3

Course Designer(s)

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70 PVL E24	Genetic Algorithms for VLSI Design	Category	L	T	P	Credit
		PE	3	0	0	3

Objectives

- To introduce the fundamental concepts of speech and audio signal processing, including signal characteristics and basic transformations.
- To explore various methods for analyzing and extracting important features from speech signals.
- To understand the principles of speech synthesis and recognition, along with their real-world applications.
- To study various techniques for processing, enhancing, and compressing audio signals.
- To explore the applications of speech and audio processing in various domains such as AI, healthcare, and telecommunications.

Prerequisite

- Nil

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Describe the basic properties of speech and audio signals and apply fundamental signal processing techniques	Understand
CO2	Discuss speech feature extraction techniques such as LPC and MFCC for speech recognition applications.	Understand
CO3	Develop basic speech recognition models and explain the working of speech synthesis systems.	Apply
CO4	Apply noise reduction and audio enhancement techniques to improve signal quality	Apply
CO5	Compare different speech and audio processing methods in real-world applications	Analyse

Mapping with Programme Outcomes

COs	POs					
	1	2	3	4	5	6
CO1	3	-	3	-	-	3
CO2	3	-	3	3	-	3
CO3	3	-	3	3	-	3
CO4	3	3	3	3	-	3
CO5	3	3	3	-	3	3
3 - Strong; 2 - Medium; 1 - Some						

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	Test 1	Test 2	
Remember	10	10	20
Understand	50	30	50
Apply	-	10	20
Analyse	-	10	10
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Syllabus

K.S.Rangasamy College of Technology – Autonomous R2025

M.E-VLSI Design

70 PVL E24 – Genetic Algorithm for VLSI Design

Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
II	3	0	2	45	3	40	60	100

Overview of Genetic Algorithms Introduction to GA Technology - Simple GA algorithm -Steady State Algorithm - Selection - Crossover - Mutation - Fitness Scaling - Inversion	[9]
Genetic Algorithm for VLSI Design GA for VLSI Design, Layout and Test automation - Partitioning - Automatic Placement - Automatic Routing - Technology mapping for FPGAs - Automatic test generation - Genetic Multiway Partitioning	[9]
Advanced Genetic Algorithms Hybrid genetic - Genetic encoding - Local improvement - WDFR - Comparison of CAs - Standard cell placement - GASP algorithm - Unified algorithm.	[9]
Genetic Algorithm for VLSI Testing Macro Cell Global routing - FPGA technology mapping - Circuit segmentation - Test generation in a GA frame work - Test generation procedures.	[9]
Applications Power estimation - Application of GA - Standard cell placement - GA for ATG - Problem Encoding - Fitness function - GA vs Conventional Algorithm.	[9]
Total Hours	**45**

Textbook(s):

1.	Pinaki Mazumder, E.MRudnick, "Genetic Algorithm for VLSI Design, Layout and test Automation", Prentice Hall, 1999
2.	Randy L. Haupt, Sue Ellen Haupt, "Practical Genetic Algorithms" 2nd Edition, John Wiley & Sons, 2004

Reference(s):

1.	Ricardo Sal Zebulum, Macro Aurelio Pacheco, Marley Maria B.R. Vellasco, Marley Maria Bernard Vellasco "Evolution Electronics: Automatic Design of electronic Circuits and Systems Genetic Algorithms", CRC press, 2001.
2.	Smith M.J.S, "Application Specific Integrated Circuits", Addison -Wesley, 2018
3.	John R.Koza, Forrest H.Bennett, David Andre, Morgan Kufmann, "Genetic Programming: Automatic Discovery of Reusable Programs", MIT Press, 1999

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Course Contents and Lecture Schedule

S. No.	Topics	No. of hours
1.0	**Overview of Genetic Algorithms**	
1.1	Introduction to GA Technology	2
1.2	Simple GA algorithm	1
1.3	Steady State Algorithm	1
1.4	Selection	1
1.5	Crossover	1
1.6	Mutation	1
1.7	Fitness Scaling	1
1.8	Inversion	1
2.0	**Genetic Algorithm for VLSI Design**	
2.1	GA for VLSI Design	1
2.2	Layout and Test automation	2
2.3	Partitioning - Automatic Placement	2
2.4	Automatic Routing	1
2.5	Technology mapping for FPGAs	1
2.6	Automatic test generation	1
2.7	Genetic Multiway Partitioning	1
3.0	**Advanced Genetic Algorithms**	
3.1	Hybrid genetic	2
3.2	Genetic encoding	1
3.3	Local improvement	1
3.4	WDFR	1
3.5	Comparison of CAs	1
3.6	Standard cell placement	1
3.7	GASP algorithm	1
3.8	Unified algorithm	1
4.0	**Genetic Algorithm for VLSI Testing**	
4.1	Macro Cell Global routing	2
4.2	FPGA technology mapping	2
4.3	Circuit segmentation	2
4.4	Test generation in a GA frame work	2
4.5	Test generation procedures	1
5.0	**Applications**	
5.1	Power estimation	2
5.2	Application of GA	2
5.3	Standard cell placement	1
5.4	GA for ATG	1
5.5	Problem Encoding	1
5.6	Fitness function	1
5.7	GA vs Conventional Algorithm	1

Course Designer(s)

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Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

70 PVL E25	Bio Signal Processing	Category	L	T	P	Credit
		PE	3	0	0	3

Objectives

- To Know the basic concept of signals and systems and their spectrums
- To analyze the Spectral estimation
- To apply the concept of adaptive filtering and their wavelets in bio signals
- To explain bio signal classification
- To Carry out multivariate component analysis

Pre-requisites

- Digital Signal Processing

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Know the characteristics basic signals, system and spectrums	Understand
CO2	Analyze the Bio signals in time domain and spectral estimation	Analyse
CO3	Analyze the Adaptive filtering and wavelet detection in ECG	Analyse
CO4	Explain bio signal classification	Understand
CO5	analyze the multivariate components in time frequency domains	Analyse

Mapping with Programme Outcomes

COs	POs					
	1	2	3	4	5	6
CO1	3	3	3	3	-	-
CO2	3	3	3	3	-	-
CO3	3	3	3	3	3	-
CO4	3	3	3	3	3	-
CO5	3	3	3	3	-	-
3 - Strong; 2 - Medium; 1 - Some						

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	20	20	20
Understand	20	20	40
Apply	10	10	20
Analyse	10	10	20
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Syllabus

K.S.Rangasamy College of Technology – Autonomous R2025

M.E-VLSI Design

70 PVL E25- Bio Signal Processing

Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
II	3	0	0	45	3	40	60	100

Signal, System and Spectrum Characteristics of Some Dynamic Biomedical Signals, Noises-Random, Structured and Physiological Noises, Filters-IIR and FIR Filters, Spectrum- Power Spectral Density Function, Cross-Spectral Density and Coherence Function, Cepstrum and Homomorphic Filtering, Estimation of Mean of Finite Time Signals.	[9]
Time Series Analysis and Spectral Estimation Time Series Analysis- Linear Prediction Models, Process Order Estimation, Non-Stationary Process, Fixed Segmentation, Adaptive Segmentation, Application in EEG, PCG and HRV Signals, Model Based ECG Simulator, Spectral Estimation-Blackman Tukey Method, Periodogram and Model Based Estimation, Application in Heart Rate Variability, PCG Signals.	[9]
Adaptive Filtering and Wavelet Detection Filtering-LMS Adaptive Filter, Adaptive Noise Cancelling in ECG, Improved Adaptive Filtering in FECG, EEG and Other Applications in Bio Signals, Wavelet Detection in ECG-Structural Features, Matched Filtering, Adaptive Wavelet Detection, Detection of Overlapping Wavelets.	[9]
Biosignal Classification and Recognition Signal Classification and Recognition- Statistical Signal Classification, Linear Discriminant Function, Direct Feature Selection and Ordering, Back Propagation Neural Network Based Classification, Application in Normal Versus Ectopic ECG Beats and Other Biomedical Applications	[9]
Time Frequency and Multivariate Analysis Time Frequency Representation, Spectrogram, Time-Scale Representation, Scalogram, Wavelet Analysis- Data Reduction Techniques, ECG Data Compression, ECG Characterization, Feature Extraction- Wavelet Packets, Multivariate Component Analysis – PCA, ICA.	[9]
Total Hours	**45**

Reference(s):

1.	Arnon Cohen, "Bio-medical Signal Processing Vol I and Vol II", CRC Press Inc., Boca Rato, Florida 2019.
2.	Emmanuvel C. Ifeachor, Barrie W.Jervis, "Digital Signal Processing-A Practical approach" , 2nd edition, Pearson education Ltd., 2002
3.	P.Ramesh Babu, "Digital Signal Processing", 6th Edition, Scitech publications, Chennai, 2014.
4.	Raguveer M.Rao and AjithS.Bopardikar, "Wavelets Transform-Introduction to theory and its Applications", Pearson Education, India 2000.
5.	Rangaraj, M.Rangayyan, "Biomedical Signal Analysis-A case study approach", Wiley, 2nd edition IEEE Press, 2015.

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Course Contents and Lecture Schedule

S. No.	Topics	No. of hours
1.0	**Signal, System and Spectrum**	
1.1	Characteristics of Some Dynamic Biomedical Signals	1
1.2	Noises-Random, Structured and Physiological Noises	1
1.3	FIR Filters	1
1.4	IIR Filters	1
1.5	Power Spectral Density function	1
1.6	Cross Spectral Density Function	1
1.7	Coherence Function	1
1.8	Cepstrum and Homomorphic Filtering	1
1.9	Estimation of Mean of Finite Time Signals	1
2.0	**Time Series Analysis and Spectral Estimation**	
2.1	Time Series Analysis, Linear Prediction Models	1
2.2	Process Order Estimation	1
2.3	Non Stationary Process	1
2.4	Fixed Segmentation and Adaptive Segmentation	1
2.5	Application in EEG, PCG and HRV Signals	1
2.6	Model Based ECG Simulator	1
2.7	Spectral Estimation, Blackman Tuckey Method	1
2.8	Periodogram and Model Based Estimation	1
2.9	Application in Heart Rate Variability, PCG Signals	1
3.0	**Adaptive Filtering and Wavelet Detection**	
3.1	Filtering, LMS Adaptive Filter	1
3.2	Adaptive Noise Cancelling in ECG	1
3.3	Improved Adaptive Filtering in FECG	1
3.4	EEG and other Applications in Bio Signals	1
3.5	Wavelet Detection in ECG	1
3.6	Structural Features	1
3.7	Matched Filtering	1
3.8	Adaptive Wavelet Detection	1
3.9	Detection of Overlapping Wavelets	1
4.0	**Biosignal Classification and Recognition**	
4.1	Signal Classification and Recognition	1
4.2	Statistical Signal Classification	1
4.3	Linear Discriminant Function	1
4.4	Direct Feature Selection and Ordering	2
4.5	Back Propagation Neural Network Based Classification	2
4.6	Application in Normal Versus Ectopic ECG Beats	1
4.7	Other Medical Applications	1
5.0	**Time Frequency and Multivariate Analysis**	
5.1	Time Frequency Representation, Spectrogram	1

5.2	Time Scale Representation,	1
5.3	Scalogram	1
5.4	Wavelet Analysis, Data Reduction Techniques	1
5.5	ECG Data Compression	1
5.6	ECG Data Characterization	1
5.7	Feature Extraction	1
5.8	Wavelet Packets	1
5.9	Multivariate Component Analysis-PCA, ICA	1

Course Designer(s)

Mr.P.Balamurugan –pbalamurugan@ksrct.ac.in

70 PVL E31	VLSI for Wireless Communication	Category	L	T	P	Credit
		PE	3	0	0	3

Objectives

- To understand the design concepts of low noise amplifiers.
- To learn the various types of mixers designed for wireless communication.
- To learn and design PLL and VCO.
- To know the concepts of data converters in communication
- To learn the concepts of CDMA in wireless communication

Pre-requisites

- Fundamentals of VLSI and Wireless Communication

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Know the concept of MOSFET and BJT Amplifier design.	Analyse
CO2	Describe the concept of Mixer	Apply
CO3	Describe the concept of frequency Synthesizers	Apply
CO4	Know the basic concept of data converters in communications.	Analyse
CO5	Describe the VLSI Implementation concept for wireless System.	Understand

Mapping with Programme Outcomes

COs	POs					
	1	2	3	4	5	6
CO1	3	3	3	3	-	3
CO2	3	3	3	3	-	3
CO3	3	3	3	3	-	3
CO4	3	2	3	3	3	3
CO5	3	2	3	3	3	3
3 - Strong; 2 - Medium; 1 - Some						

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	20	20	20
Understand	10	10	20
Apply	20	20	50
Analyse	10	10	10
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Syllabus

K.S.Rangasamy College of Technology – Autonomous R2025

M.E-VLSI Design

70 PVL E31- VLSI for Wireless Communication

Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
II	3	0	0	45	3	40	60	100

Components and Devices Integrated Inductors- Resistors- MOSFET and BJT Amplifier Design: Low Noise Amplifier Design – Wideband LNA - Design Narrowband LNA - Impedance Matching-Matching of Imaginary and Real Part-Interpretation of Power Matching - Automatic Gain Control Amplifiers — Power Amplifiers.	[9]
Mixers Balancing Mixer - Qualitative Description of the Gilbert Mixer - Conversion Gain — Distortion – Low Frequency Case: Analysis of Gilbert Mixer – Distortion - High-Frequency Case — Noise — A Complete Active Mixer. Switching Mixer - Distortion in Unbalanced Switching Mixer – Conversion Gain in Unbalanced Switching Mixer - Noise in Unbalanced Switching Mixer - A Practical Unbalanced Switching Mixer - Sampling Mixer - Conversion Gain in Single Ended Sampling Mixer - Distortion in Single Ended Sampling Mixer - Intrinsic Noise in Single Ended Sampling Mixer - Extrinsic Noise in Single Ended Sampling Mixer.	[9]
Frequency Synthesizers Phase Locked Loops - Voltage Controlled Oscillators - Phase Detector – Analog Phase Detectors — Digital Phase Detectors - Frequency Dividers - LC Oscillators - Ring Oscillators - Phase Noise - A Complete Synthesizer Design Example (DECT Application).	[9]
Sub Systems Data Converters in Communications - Adaptive Filters - Equalizers and Transceivers	[9]
Implementations VLSI Architecture for Multitier Wireless System - Hardware Design Issues for a Next Generation CDMA System	[9]
Total Hours	**45**

Text book(s):

1	B.Razavi , "RF Microelectronics" , 2nd Edition Prentice Hall of India Private Ltd.,2013.
2	Bosco H. Leung, "VLSI for Wireless Communication", 2nd Edition, Springer US, 2014.

Reference(s):

1.	Lee,Thomas H.Lee, "The Design of CMOS Radio Frequency Integrated Circuits", 2nd Edition, Cambridge University Press, 2013.
2.	Emad N Farag, Mohamed I. Elmasry " Mixed Signal VLSI Wireless Design: Circuits and Systems", Springer US, 2013.
3.	BehzadRazavi, "Design of Analog CMOS Integrated Circuits", Tata McGraw Hill, 2012.
4.	J. Crols and M. Steyaert, "CMOS Wireless Transceiver Design", Springer, 2013.

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Course Contents and Lecture Schedule		
S. No.	**Topics**	**No. of hours**
1.0	**Components and Devices**	
1.1	Integrated Inductors- Resistors	1
1.2	MOSFET and BJT Amplifier Design	1
1.3	Low Noise Amplifier Design	1
1.4	Wideband LNA - Design Narrowband LNA	1
1.5	Impedance Matching-Matching of Imaginary	1
1.6	Real Part-Interpretation of Power Matching	1
1.7	Automatic Gain Control Amplifiers	1
1.8	Power Amplifiers	1
2.0	**Mixers**	
2.1	Balancing Mixer - Qualitative Description of the Gilbert Mixer - Conversion Gain — Distortion	1
2.2	Low Frequency Case: Analysis of Gilbert Mixer	1
2.3	Distortion - High-Frequency Case – Noise – A Complete Active Mixer	1
2.4	Switching Mixer - Distortion in Unbalanced Switching Mixer –	1
2.5	Conversion Gain in Unbalanced Switching Mixer	1
2.6	Noise in Unbalanced Switching Mixer - A Practical Unbalanced Switching Mixer	1
2.7	Sampling Mixer - Conversion Gain in Single Ended Sampling Mixer	1
2.8	Distortion in Single Ended Sampling Mixer - Intrinsic Noise in Single Ended Sampling Mixer	1
2.9	Extrinsic Noise in Single Ended Sampling Mixer.	1
3.0	**Frequency Synthesizers**	
3.1	Phase Locked Loops - Voltage Controlled Oscillators	1
3.2	Phase Detector – Analog Phase Detectors	2
3.3	Digital Phase Detectors - Frequency Dividers	2
3.4	LC Oscillators - Ring Oscillators	1
3.5	Phase Noise	2
3.6	A Complete Synthesizer Design Example (DECT Application).	1
4.0	**Sub Systems**	
4.1	Introduction to Subsystems	1
4.2	Data Converters	1
4.3	Data Converters in Communications (Analog)	1
4.4	Data Converters in Communications (Digital)	2
4.5	Adaptive Filters	2
4.6	Equalizers	1
4.7	Transceivers	1
5.0	**Implementations**	
5.1	Introduction	2
5.2	VLSI Architecture for Multitier Wireless System	3
5.3	Introduction to CDMA	2
5.4	Hardware Design Issues for a Next generation CDMA System	2

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Course Designer(s)

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Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

70 PVL E32	System on Chip	Category	L	T	P	Credit
		PE	3	0	0	3

Objectives

- To design combinational and sequential logic networks.
- To learn optimization of power in combinational and sequential logic machines.
- To study the design principles of FPGA and PLA.
- To learn various floor planning methods for system design.
- To understand and apply floor-planning techniques, including block placement, routing, power and clock distribution, and off-chip connections for optimized VLSI design.

Pre-requisites

- Nil

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Design combinational and sequential logic networks.	Apply
CO2	Learn optimization of power in combinational and sequential logic machines	Analyse
CO3	Outline the design principles of FPGA and PLA.	Understand
CO4	Learn various floor planning methods for system design.	Understand
CO5	Understand and apply floor-planning techniques, including block placement, routing, power and clock distribution, and off-chip connections for optimized VLSI design.	Apply

Mapping with Programme Outcomes

COs	POs					
	1	2	3	4	5	6
CO1	3	3	3	2	2	2
CO2	3	2	3	2	2	2
CO3	2	2	3	2	2	2
CO4	2	2	3	2	2	2
CO5	3	3	3	2	3	3
3 - Strong; 2 - Medium; 1 - Some						

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	12	20	20
Understand	28	40	50
Apply	10	-	20
Analyse	10	-	10
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

Syllabus

K.S.Rangasamy College of Technology – Autonomous R2025								
M.E-VLSI Design								
70 PVL E32- System on Chip								
Semester	**Hours/Week**			**Total Hours**	**Credit**	**Maximum Marks**		
	L	T	P		C	CA	ES	Total
II	3	0	0	45	3	40	60	100

Logic Gates Introduction. Combinational Logic Functions. Static Complementary Gates. Switch Logic. Alternative Gate Circuits. Low-Power Gates. Delay Through Resistive Interconnect. Delay Through Inductive Interconnect. Objectives	[9]
Combinational Logic Networks Introduction. Standard Cell-Based Layout. Simulation. Combinational Network Delay. Logic and interconnect Design. Power Optimization. Switch Logic Networks. Combinational Logic Testing.	[9]
Sequential Machines Introduction. Latches and Flip-Flops. Sequential Systems and Clocking Disciplines. Sequential System Design. Power Optimization. Design Validation. Sequential Testing.	[9]
Subsystem Design Introduction. Subsystem Design Principles. Combinational Shifters. Adders. ALUs. Multipliers. High-Density Memory. Field Programmable Gate Arrays. Programmable Logic Arrays.	[9]
Floor-Planning Introduction, Floor-planning Methods — Block Placement & Channel Definition, Global Routing, switchbox Routing, Power Distribution, Clock Distributions, Floor-planning Tips, Design Validation. Off-Chip Connections — Packages, The I/O Architecture, PAD Design.	[9]
Total Hours	45
Text Book(s):	

1.	Neil H. E. Weste, David Harris, "CMOS VLSI Design: A Circuits and Systems Perspective",2019
2.	Jan M. Rabaey,"Digital Integrated Circuits: A Design Perspective", 2020
3.	Neil H. E. Weste, "Principles of CMOS VLSI Design", Kamran Eshraghian

References(s):

1.	Wayne Wolf, “Modern VLSI Design – System – on – Chip Design”, Prentice Hall, 3rd Edition, 2008.
2.	Wayne Wolf , “Modern VLSI Design – IP based Design”, Prentice Hall, 4th Edition, 2008.

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Course Contents and Lecture Schedule

S. No.	Topics	No. of hours
1	**Logic Gates**	
1.1	Introduction to Logic Gates	1
1.2	Combinational Logic Functions	2
1.3	Static Complementary Gates & Switch Logic	2
1.4	Alternative Gate Circuits & Low-Power Gates	2
1.5	Delay Through Resistive & Inductive Interconnect	2
2	**Combinational Logic Networks**	
2.1	Introduction & Standard Cell-Based Layout	2
2.2	Simulation & Combinational Network Delay	2
2.3	Logic and Interconnect Design	2
2.4	Power Optimization & Switch Logic Networks	2
2.5	Combinational Logic Testing	1
3	**Sequential Machines**	
3.1	Introduction to Sequential Machines	1
3.2	Latches and Flip-Flops	1
3.3	Sequential Systems and Clocking Disciplines	2
3.4	Sequential System Design	2
3.5	Power Optimization	1
3.6	Design Validation	1
3.7	Sequential Testing	1
3.8	Practical Implementation & Simulation	
4	**Subsystem Design**	
4.1	Introduction to Subsystem Design Principles	1
4.2	Combinational Shifters	1
4.3	Adders	1
4.4	ALUs	1
4.5	Multipliers	1
4.6	High-Density Memory	1
4.7	Field Programmable Gate Arrays (FPGAs)	1
4.8	Programmable Logic Arrays (PLAs)	2
5	**Floor-Planning**	
5.1	Introduction to Floor-Planning	2
5.2	Floor-Planning Methods: Block Placement & Channel Definition	2
5.3	Global Routing	1
5.4	Switchbox Routing	1
5.5	Power Distribution & Clock Distributions	1
5.6	Floor-Planning Tips & Design Validation	1

Course Designer(s)

Ms.Kausalya.S- kausalya@ksrct.ac.in

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

70 PVL E33	Design and Verification Using UVM	Category	L	T	P	Credit
		PE	3	0	0	3

Objectives

- To provide the students, a complete understanding on UVM testing
- To become proficient at UVM verification
- To Know about the verification components used and to build it
- To describe the register layer classes and to generate it
- To learn all peripheral bus test benches and its advanced level.

Pre-requisites

- System Verilog

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Understand the basic concepts of two methodologies UVM	Analyse
CO2	Build actual verification components	Apply
CO3	Generate the register layer classes	Apply
CO4	Code test benches using UVM	Apply
CO5	Understand advanced peripheral bus test benches	Apply

Mapping with Programme Outcomes

COs	POs					
	1	2	3	4	5	6
CO1	3	-	3	2	1	-
CO2	3	-	3	2	2	3
CO3	3	-	3	2	2	-
CO4	3	-	3	2	2	3
CO5	3	-	3	2	2	3
3 - Strong; 2 - Medium; 1 - Some						

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	10	20	30
Understand	30	20	10
Apply	20	20	30
Analyse	-	-	30
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Syllabus

K.S.Rangasamy College of Technology – Autonomous R2025								
M.E-VLSI Design								
70 PVL E33- Design and Verification Using UVM								
Semester	**Hours/Week**			**Total Hours**	**Credit**	**Maximum Marks**		
	L	T	P		C	CA	ES	Total
II	3	0	0	45	3	40	60	100

Introduction Overview- The Typical UVM Testbench Architecture- The UVM Class Library-Transaction-Level Modelling (TLM) -Overview- TLM, TLM-1, and TLM-2.0 -TLM-1 Implementation- TLM-2.0 Implementation.	[9]
Developing Reusable Verification Components* Modelling Data Items for Generation - Transaction-Level Components - Creating the Driver – Creating the Sequencer - Connecting the Driver and Sequencer -Creating the Monitor - Instantiating Components- Creating the Agent - Creating the Environment -Enabling Scenario Creation -Managing of Test-Implementing Checks and Coverage	[9]
UVM using Verification Components Creating a Top-Level Environment- Instantiating Verification Components - Creating Test Classes - Verification Component Configuration - Creating and Selecting a User-Defined Test – Creating Meaningful Tests- Virtual Sequences- Checking for DUT Correctness- Scoreboards- Implementing a Coverage Model	[9]
UVM using the Register Layer Classes** Using the Register Layer Classes - Back-Door Access -Special Registers -Integrating a Register Model in a Verification Environment- Integrating a Register Model- Randomizing Field Values- Pre-Defined Sequences	[9]
Assignment in Test benches Assignment, APB: Protocol, Test bench Architecture, Driver and Sequencer, Monitor, Agent and Env; Creating Sequences, Building Test, Design and Testing of Top Module.	[9]
Total Hours	**45**

Text book(s):	
1	https://www.accellera.org/images/downloads/standards/uvm/uvm_users_guide_1.1.pdf
2	https://www.udemy.com/course/learn-ovm-uvm/
Reference(s):	
1.	http://www.testbench.in/ut_00_index.html
2.	http://www.testbench.in/ot_00_index.html

*SDG 4 – Quality Education
**SDG 9 – Industry, Innovation, and Infrastructure

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Course Contents and Lecture Schedule		
S. No.	**Topics**	**No. of hours**
1	**Introduction to UVM**	
1.1	Overview	1
1.2	Typical UVM Testbench Architecture	1
1.3	UVM Class Library	1
1.4	Transaction-Level Modeling - Overview	1
1.5	TLM, TLM-1	2
1.6	TLM-2.0	1
1.7	TLM-1 Implementation	1
1.8	TLM-2.0 Implementation	1
2	**Developing Reusable Verification Components**	
2.1	Modeling Data Items for Generation	1
2.2	Transaction-Level Components	1
2.3	Creating the Driver	1
2.4	Creating the Sequencer	1
2.5	Connecting the Driver and Sequencer, Creating the Monitor	1
2.6	Instantiating Components, Creating the Agent	1
2.7	Creating the Environment	1
2.8	Enabling Scenario Creation	1
2.9	Managing of Test-Implementing Checks and Coverage	
3	**UVM Using Verification Components**	
3.1	Creating a Top-Level Environment	1
3.2	Instantiating Verification Components	1
3.3	Creating Test Classes	1
3.4	Verification Component Configuration	1
3.5	Creating and Selecting a User-Defined Test	1
3.6	Creating Meaningful Tests- Virtual Sequences	1
3.7	Checking for DUT Correctness	1
3.8	Scoreboards	1
3.9	Implementing a Coverage Model	1
4	**UVM using the Register Layer Classes**	
4.1	Using the Register Layer Classes	1
4.2	Back-Door Access	1
4.3	Special Registers	1
4.4	Integrating a Register Model in a Verification Environment	2
4.5	Integrating a Register Model	2
4.6	Randomizing Field Values	1
4.7	Pre-Defined Sequences	1
5	**Assignment in Test benches**	
5.1	Assignment	1
5.2	APB: Protocol	1
5.3	Test bench Architecture	1
5.4	Driver and Sequencer	1
5.5	Monitor, Agent and Env	1
5.6	Creating Sequences	1
5.7	Building Test	1
5.8	Design and Testing of Top Module	2

Passed in BoS Meeting held on 13/06/2025
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Course Designer(s)

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Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

70 PVL E34	FPGA Based Implementation of Signal Processing Systems	Category	L	T	P	Credit
		PE	3	0	0	3

Objectives

- To learn the basics of FPGAs and DSP systems.
- To learn the different types of FPGA technologies.
- To understand the architectures and tools for FPGA based DSP systems.
- To know the concepts of IP cores and implementation for FPGA DSP systems.
- To learn low power FPGA Implementation

Pre-requisites

- Digital Logic Design and Digital Signal Processing

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Know the fundamental of FPGAs and computer arithmetic unit of DSP systems	Understand
CO2	Analyze various FPGA technologies and implementation for DSP systems	Apply
CO3	Know the design requirements, concept and tools for FPGA based DSP architectures	Apply
CO4	Learn the concept of IP cores for FPGA complex DSP systems	Understand
CO5	Explain the power reduction techniques and architecture for low power FPGA implementation and application of FFT in VLSI	Understand

Mapping with Programme Outcomes

COs	POs					
	1	2	3	4	5	6
CO1	3	3	3	3	-	3
CO2	3	3	3	3	-	3
CO3	3	3	3	3	3	3
CO4	3	3	3	3	3	3
CO5	3	3	3	3	-	3
3 - Strong; 2 - Medium; 1 - Some						

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	20	10	30
Understand	10	30	30
Apply	30	20	40
Analyse	-	-	-
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Syllabus

K.S.Rangasamy College of Technology – Autonomous R2025								
M.E-VLSI Design								
70 PVL E34- FPGA Based Implementation of Signal Processing Systems								
Semester	**Hours/Week**			**Total Hours**	**Credit**	**Maximum Marks**		
	L	T	P		C	CA	ES	Total
II	3	0	0	45	3	40	60	100

Fundamentals of FPGAs and DSP Introduction to Field-Programmable Gate Arrays, a Short History of the Microchip, Influence of Programmability, Challenges of FPGAs, DSP System Basics, DSP System Definitions, DSP Transforms, Filter Structures, Adaptive Filtering, Basics of Adaptive Filtering, Number Systems, Fixed-Point and Floating-Point, Arithmetic Operations, Fixed-Point Versus Floating-Point.	[9]
FPGA Technologies and Implementation Issues Xilinx FPGA Technologies, Altera FPGA Technologies, Various Forms of the LUT, Memory Availability Fixed Coefficient Design Techniques, Distributed Arithmetic, Reduced Coefficient Multiplier	[9]
Architectures and Tools for FPGA Based DSP Systems The Evolution of FPGA System Design, Design Methodology Requirements for FPGA DSP, System Specification, IP Core Generation Tools for FPGA, System-level Design Tools for FPGA, DSP Algorithm Characteristics, DSP Algorithm Representations, Basics of Mapping DSP Systems onto FPGAs, Parallel Operation, Hardware Sharing, Application to FPGA.	[9]
Complex DSP Systems* Motivation for Design for Reuse, Intellectual Property (IP) Cores, Evolution of IP Cores, Parameterizable (Soft) IP Cores, IP Core Integration, IP Core Example, Current FPGA-based IP Cores, Dataflow Modeling and Rapid Implementation for FPGA DSP Systems, System-level Design and Exploration of Dedicated Hardware.	[9]
Low Power FPGA Implementation** Sources of Power Consumption, Power Consumption Reduction Techniques, Voltage Scaling in FPGAs, Reduction in Switched Capacitance, Data Reordering, Fixed Coefficient Operation, Pipelining, Locality, Application to an FFT Implementation, Reconfigurable Systems, Memory Architectures, Support for Floating- point Arithmetic.	[9]
Total Hours	**45**

Text book(s):	
1	Roger Woods, John McAllister, Gaye Light body and Ying Yi, "FPGA-based Implementation of Signal Processing Systems",2nd Edition, John Wiley and Sons, 2017.
2	Wayne Wolf, "FPGA-Based System Design", Prentice Hall, New Delhi, 2012.
Reference(s):	
1.	Uwe Meyer Baese,"Digital Signal Processing with Field Programmable Gate Arrays", 4th Edition, Springer, 2016.
2.	Neil H.E.Weste, Kamran Eshraghian, "Principles of CMOS VLSI Design", 2nd Edition, Pearson, 2018.
3.	John G.Proakis, Dimitris Manolakis, "Digital Signal Processing: Principles, Algorithms and Applications", 4th Edition, Pearson Education, 2014.
4.	Sanjit K.Mitra, "Digital Signal Processing: A Computer based approach", 4th Edition, McGraw-Hill, 2013.

* SDG 9 – Industry, Innovation, and Infrastructure
**SDG 7 – Affordable and Clean Energy

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Course Contents and Lecture Schedule		
S. No.	**Topics**	**No. of hours**
1.0	**Fundamentals of FPGAs and DSP**	
1.1	Introduction to Field-programmable Gate Arrays	1
1.2	A Short History of the Microchip, Influence of Programmability,	1
1.3	Challenges of FPGAs	1
1.4	DSP System Basics, DSP System Definitions	1
1.5	DSP Transforms,	1
1.6	Filter Structures,	1
1.7	Adaptive Filtering, Basics of Adaptive Filtering	1
1.8	Number Systems, Fixed-point and Floating-point	1
1.9	Arithmetic Operations, Fixed-point versus Floating-point	1
2.0	**FPGA Technologies and Implementation Issues**	
2.1	Xilinx FPGA Technologies	2
2.2	Altera FPGA Technologies	2
2.3	Various Forms of the LUT	2
2.4	Memory Availability Fixed Coefficient Design Techniques	1
2.5	Distributed Arithmetic	1
2.6	Reduced Coefficient Multiplier	1
3.0	**Architectures and Tools for FPGA Based DSP Systems**	
3.1	The Evolution of FPGA System Design	1
3.2	Design Methodology Requirements for FPGA DSP	1
3.3	System Specification, IP Core Generation Tools for FPGA	1
3.4	System-level Design Tools for FPGA	1
3.5	DSP Algorithm Characteristics	1
3.6	DSP Algorithm Representations	1
3.7	Basics of Mapping DSP Systems onto FPGAs	1
3.8	Parallel Operation	1
3.9	Hardware Sharing, Application to FPGA	1
4.0	**Complex DSP systems**	
4.1	Motivation for Design for Reuse	1
4.2	Intellectual Property (IP) Cores	1
4.3	Evolution of IP Cores, Para meterizable (Soft) IP Cores	1
4.4	Para meterizable (Soft) IP Cores	1
4.5	IP Core Integration, IP Core Example	1
4.6	Current FPGA-based IP Cores	1
4.7	Data flow Modeling and Rapid Implementation for FPGA DSP Systems	1
4.8	System-level Design	1
4.9	Exploration of Dedicated Hardware	1
5.0	**Low Power FPGA Implementation**	
5.1	Sources of Power Consumption	1
5.2	Power Consumption Reduction Techniques	1
5.3	Voltage Scaling in FPGAs	1
5.4	Reduction in Switched Capacitance	1
5.5	Data Reordering	1
5.6	Fixed Coefficient Operation	1

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5.7	Pipelining, Locality	1
5.8	Application to an FFT Implementation, Reconfigurable Systems	1
5.9	Reconfigurable Systems, Memory Architectures, Support for Floating- point Arithmetic.	1

Course Designer(s)

Mr.P.Balamurugan – pbalamurugan@ksrct.ac.in

70 PVL E35	Wireless Sensor Networks	Category	L	T	P	Credit
		PE	3	0	0	3

Objectives

- To understand the fundamental concepts and architecture of Wireless Sensor Networks (WSN)
- To acquire knowledge of various routing protocols used in WSN
- To explore the principles and applications of 6LoWPAN technology
- To gain insight into operating systems designed for WSN environments
- To enhance understanding of operating systems specific to 6LoWPAN-based networks.

Pre-requisites

- Nil

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Examine the architecture and design principles of Wireless Sensor Networks (WSNs)	Understand
CO2	Identify the functionalities and characteristics of various routing protocols used in WSNs	Understand
CO3	Outline the 6LoWPAN architecture and explain header compression techniques	Understand
CO4	Implement suitable protocols for various types of sensor networks based on their functionality and requirements.	Apply
CO5	Develop functional modules and apply operating systems commonly used in wireless sensor networks	Apply

Mapping with Programme Outcomes

COs	POs					
	1	2	3	4	5	6
CO1	3	3	3	-	-	3
CO2	3	3	3	-	-	3
CO3	3	3	3	-	-	3
CO4	3	3	3	-	-	3
CO5	3	3	3	-	3	3
3 - Strong; 2 - Medium; 1 - Some						

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	20	-	20
Understand	40	40	30
Apply	-	20	50
Analyse	-	-	-
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Syllabus

K.S.Rangasamy College of Technology – Autonomous R2025

M.E-VLSI Design

70 PVL E35- Wireless Sensor Networks

Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
II	3	0	0	45	3	40	60	100

Wireless Sensor Network Architecture* Challenges - Comparison with Ad hoc Network - Node Architecture and Network Architecture - Design Principles - Short Range Radio Communication Standards - IEEE 802.15.4 - Zigbee and Bluetooth- Energy Harvesting Techniques for WSN nodes.	[9]
Routing Protocols* Fundamentals - Low Duty Cycle and Wakeup Concepts - Routing protocols - Requirements - Classification - SPIN - Directed Diffusion – LEACH – PEGASIS- EAR (Energy-Aware Routing) – EADR (Energy-Aware Distance Routing)	[9]
6LoWPAN* 6LoWPAN Architecture - Protocol Stack - Adaptation Layer - Link layers – Routing - Mesh - Under - Route - Over - Header Compression - Stateless Header Compression - Context - Based Header Compression - Mobility - Mobile IPv6, Proxy Home Agent - Proxy MIPv6 - Security Considerations in 6LoWPAN	[9]
Application* Design Issues - Real-Time Streaming and Sessions - Publish/Subscribe - Web Service Paradigms - Common Protocols - Web Service Protocols, MQ Telemetry Transport for Sensor Networks (MQTT-S) - ZigBee Compact Application Protocol (CAP)- WSNs in Healthcare	[9]
Sensor Network Platforms TinyOS - NesC - Interfaces - Modules - Configuration - Programming in TinyOS using NesC. TOSSIM - Simulation Environment - Cooja Simulator, Programming.	[9]
Total Hours	**45**

Text book(s):

1	Holger Karl, Andreas Willig, “Protocol and Architecture for Wireless Sensor Networks”, John Wiley & Sons 2007.
2	Anna Forster, “Introduction to Wireless Sensor Networks”, Wiley, 2017.

Reference(s):

1.	Hongmei Deng, Wei Li and Dharma P. Agrawal, “Routing security in Wireless Ad hoc Networks", IEEE Communication Magazine, 2002.
2.	Zach Shelby Sensinode and Carsten Bormann, “6LoWPAN: The Wireless Embedded Internet” John Wiley and Sons, 2009.
3.	Philip Levis, “TinyOS Programming”, 2006 –www.tinyos.net.
4.	The Contiki Operating System.http://www.sics.se/Contiki.

*SDG4 Quality Education

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Course Contents and Lecture Schedule		
S. No.	**Topics**	**No. of hours**
1.0	**Wireless Sensor Network Architecture**	
1.1	Challenges	1
1.2	Comparison with Ad hoc Network	1
1.3	Node Architecture	1
1.4	Network Architecture	1
1.5	Design Principles	1
1.6	Short Range Radio Communication standards	1
1.7	Zigbee	1
1.8	Bluetooth	1
1.9	Energy Harvesting Techniques for WSN nodes	1
2.0	**Routing Protocols**	
2.1	Fundamentals, Low Duty Cycle Protocols	1
2.2	Wakeup Concepts	1
2.3	Routing Protocols – Requirements	1
2.4	SPIN	1
2.5	Directed Diffusion	1
2.6	LEACH	1
2.7	PEGASIS	1
2.8	EAR	1
2.9	EADR	1
3.0	**6LoWPAN**	
3.1	6LoWPAN Architecture, Protocol Stack	1
3.2	Adaptation Layer	1
3.3	Link layers, Addressing	1
3.4	Routing - Mesh-Under- Route-Over	1
3.5	Header Compression - Stateless Header Compression	1
3.6	Context- Based Header Compression	1
3.7	Fragmentation and Reassembly	1
3.8	Mobile Ipv6, Proxy Home Agent	1
3.9	Security Considerations in 6LoWPAN	1
4.0	**Application**	
4.1	Design Issues, Real-Time Streaming	1
4.2	Sessions Publish/Subscribe	1
4.3	Web Service Paradigms	1
4.4	Common Protocols	1
4.5	Web Service Protocols	1
4.6	MQ Telemetry Transport for Sensor Networks (MQTT-S)	2
4.7	Zigbee Compact Application Protocol (CAP)	1
4.8	WSNs in Healthcare	1
5.0	**Sensor Network Platforms**	
5.1	Tinyos	1
5.2	Nesc Interfaces	1

5.3	Modules, Configuration	1

5.4	Programming in Tinyos Using Nesc	1
5.5	TOSSIM	1
5.6	Simulation Environment - Cooja Simulator	2
5.7	Simulation Environment – Programming	2

Course Designer(s)

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70 PAC 002	Disaster Management	Category	L	T	P	Credit
		AC	2	0	0	0

Objectives

- Summarize basics of disaster
- Explain a critical understanding of key concepts in disaster risk reduction and humanitarian response.
- Illustrate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.
- Describe an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.
- Develop the strengths and weaknesses of disaster management approaches Teach how to improve writing skills and level of readability

Pre-requisites

- Nil

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Summarize basics of disaster	Remember
CO2	Explain a critical understanding of key concepts in disaster risk reduction and humanitarian response.	Understand
CO3	Illustrate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.	Understand
CO4	Describe an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.	Understand
CO5	Develop the strengths and weaknesses of disaster management approaches	Apply

Mapping with Programme Outcomes

COs	POs					
	1	2	3	4	5	6
CO1	3	3	3	-	3	-
CO2	3	3	3	-	3	-
CO3	3	3	3	-	3	-
CO4	3	3	3	-	3	-
CO5	3	3	3	-	3	-
3 - Strong; 2 - Medium; 1 - Some						

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)	
	1	2
Remember	50	50
Understand	50	50
Apply	-	-
Analyse	-	-
Evaluate	-	-
Create	-	-
Total	100	100

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Syllabus

K.S.Rangasamy College of Technology – Autonomous R2025

Common to all Branches

60 PAC 002 – Disaster Management

Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
II	2	0	0	30	0	100	-	100

Introduction Disaster: Definition, Factors and Significance; Difference between Hazard and Disaster; Natural and Manmade Disasters: Difference, Nature, Types and Magnitude.	[6]
Repercussions of Disasters and Hazards Economic Damage, Loss of Human and Animal Life, Destruction of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts and Famines, Landslides and Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks and Spills, Outbreaks of Disease and Epidemics, War and Conflicts.	[6]
Disaster Prone Areas in India* Study of Seismic Zones; Areas Prone to Floods and Droughts, Landslides and Avalanches; Areas Prone to Cyclonic and Coastal Hazards with Special Reference to Tsunami; Post-Disaster Diseases and Epidemics	[6]
Disaster Preparedness and Management** Preparedness: Monitoring of Phenomena Triggering a Disaster or Hazard; Evaluation of Risk: Application of Remote Sensing, Data from Meteorological and other Agencies, Media Reports: Governmental and Community Preparedness.	[6]
Risk Assessment Disaster Risk: Concept and Elements, Disaster Risk Reduction, Global and National Disaster Risk Situation. Techniques of Risk Assessment, Global Co-Operation in Risk Assessment and Warning, People's Participation in Risk Assessment. Strategies for Survival.	[6]
Total Hours	**30**

Text book(s):

1	Goel S. L, "Disaster Administration and Management Text and Case Studies", Deep & Deep Publication Pvt. Ltd., New Delhi,2009.
2	Nishitha Rai, Singh AK, "Disaster Management in India: Perspectives, issues and strategies "'New Royal book Company,2007.

Reference(s):

1.	Sahni, Pardeep et.al.," Disaster Mitigation Experiences and Reflections", Prentice Hall of India, 2001.
2.	Subramanian R,"Disaster Management", Vikas publishing Housing Pvt. Ltd., 2018.
3.	Chu-hua Kuei, Christian N Madu, Handbook of Disaster Management Risk Reduction & Management: Climate change and Natural Disaster, world scientific, 2017.
4.	Janki Andharia, Disaster studies: Exploring Intersectional ties in Disaster Discourse, Springer, 2020.

*SDG 11 – Sustainable Cities and Communities
**SDG 13 – Climate Action

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

70 PVL 2P1	VLSI Laboratory II	Category	L	T	P	Credit
		PC	0	0	4	2

Objectives

- To learn the concept of System Verilog HDL
- To help engineers understand, and maintain digital hardware models and conventional verification test benches written in System Verilog.
- To provide a critical language foundation for more advanced training on System Verilog
- To develop Verilog test environments using EDA tools
- To learn the features and capabilities of the UVM class library for system Verilog

Pre-requisites

- Basic Verilog HDL

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Use the System Verilog, to design and synthesis features of digital circuits	Analyse
CO2	Appreciate and apply the System Verilog verification features, including classes, constrained random stimulus, coverage, strings, queues and dynamic arrays, and learn how to utilize these features for more effective and efficient verification.	Analyse
CO3	Implement higher level of abstraction to design and verification	Analyse
CO4	Develop Verilog test environments of significant capability and complexity	Analyse
CO5	Integrate scoreboards, multichannel sequencers and Register Models	Analyse

Mapping with Programme Outcomes

COs	POs					
	1	2	3	4	5	6
CO1	3	-	3	3	3	3
CO2	3	-	3	3	3	3
CO3	3	-	3	3	3	3
CO4	3	-	3	3	3	3
CO5	3	-	3	3	3	3
3 - Strong; 2 - Medium; 1 - Some						

Assessment Pattern

Bloom's Category	Lab Experiments Assessment (Marks)		Model Examination (Marks)	End Sem Examination (Marks)
	Lab	Activity		
Remember	-	-	-	-
Understand	-	-	20	20
Apply	50	25	80	80
Analyse	-	-	-	-
Evaluate	-	-	-	-
Create	-	-	-	-
Total	50	25	100	100

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

K.S.Rangasamy College of Technology – Autonomous R2025								
M.E-VLSI Design								
70 PVL 2P1 – VLSI Laboratory II								
Semester	**Hours/Week**			**Total Hrs**	**Credit**	**Maximum Marks**		
	L	T	P		C	CA	ES	Total
II	0	0	4	60	2	60	40	100

List of Experiments:

1. Introduction to System Verilog and UVM
2. Modeling Combinational circuits using System Verilog
3. Design FIFO using system Verilog
4. Design on FSM using system Verilog
5. Use an interface between testbench and DUT
6. Developing a test program using system Verilog
7. Create a scoreboard using dynamic array
8. Use mailboxes for verification
9. Generate constrained random test values
10. Using coverage with constrained random tests

Course Designer(s)

Mr.S.Saravanan – saravanan.s@ksrct.ac.in

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

70 PVL 2P2	Term Paper and Seminar	Category	L	T	P	Credit
		CG	0	0	2	0

Objectives

- Students will develop their scientific and technical reading and writing skills that they need to understand and construct research articles.
- A term paper requires a student to obtain information from a variety of sources (i.e., Journals, dictionaries, reference books) and then place it in logically developed ideas.
- To identify the recent topics in the research area and formulate the problem
- To analyze the mathematical model for the identified problem
- To design and simulate/ develop prototype model

Pre-requisites

- Nil

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Survey the relevant bibliography such as national/international referred journals for the preferred areas of research	Analyse
CO2	Develop scientific, technical reading and writing skills for the technical report preparation to apply it in their topics of research	Apply
CO3	Apply mathematical ideas to any problem in the research field	Apply
CO4	Implement and analyze the various complex problems in different practical applications	Analyse
CO5	Cultivate presentation skills to deliver their work in front of technically qualified audience	Apply

Mapping with Programme Outcomes

COs	1	2	3	4	5	6
CO1	3	3	3	2	3	-
CO2	3	3	3	2	3	3
CO3	3	-	3	3	-	3
CO4	3	2	3	3	2	3
CO5	3	3	3	2	3	-
3 - Strong; 2 - Medium; 1 - Some						

Assessment Pattern

Bloom's Category	Lab Experiments Assessment (Marks)	Model Examination (Marks)	End Sem Examination (Marks)
Remember	-	-	No End Semester Examination
Understand	-	-	
Apply	25	50	
Analyse	25	50	
Evaluate	-	-	
Create	-	-	
Total	50	100	

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

K.S.Rangasamy College of Technology – Autonomous R2025								
M.E-VLSI Design								
70 PVL 2P2 – Term Paper and Seminar								
Semester	**Hours/Week**			**Total Hrs**	**Credit**	**Maximum Marks**		
	L	T	P		C	CA	ES	Total
II	0	0	2	30	0	100	-	100

The work involves the following steps:

1. Selecting a subject, narrowing the subject into a topic.
2. Stating an objective.
3. Collecting the relevant bibliography (at least 15 journal papers)
4. Preparing a working outline.
5. Studying the papers and understanding the authors contributions and critically analysing each paper.
6. Preparing a working outline.
7. Linking the papers and preparing a draft of the paper.
8. Preparing conclusions based on the reading of all the papers.
9. Writing the Final Paper and giving final Presentation

Please keep a file where the work carried out by you is maintained.

Activities to be carried out

Activity	**Instructions**	**Submission week**	**Evaluation**
Selection of area of interest and Topic Stating an Objective	An area of interest, topic has to be selected and objective to be framed	2nd week	**3%** Based on clarity of thought, current relevance and clarity in writing
Collecting Information about chosen area & topic	The following details related to the chosen area must be collected. 1. List 1 special interest groups or professional society 2. List 2 journals 3. List 3 conferences, symposia or workshops 4. List1+ thesis title 5. List 5 web presences (mailing lists, forums, news sites) 6. List 6 authors who publish regularly in your area 7. Attach a call for papers (CFP) from conference/Journal/Symposium in the chosen area.	3rd week	**3%** (the selected information must be area specific and of international and national standard)
Collection of Journal papers in the topic in the context of the objective — collect 20 &	• Provide a complete list of references you will be using- Based on the objective - Search Various digital libraries and Google Scholar	4th week	**6%** (the list of standard papers and reason for selection)

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Approved in Academic Council Meeting held on 19/07/2025

then filter	• When picking papers to read - try to: • Pick papers that are related to each other in some way and/or that are in the same field so that a meaningful survey can be Written • Favour papers from well-known journals and conferences, • Favour 'first' or 'foundational' papers in the field (as indicated in other people's survey paper), Favour more recent papers, • Pick a recent survey of the field to quickly gain an overview, • Find relationships with respect to each other and to your topic area (classification scheme/categorization) • Mark in the hard copy of papers whether complete work or section/sections of the paper are being considered		
Reading and notes for first 5 papers	Reading Paper Process • For each paper form a Table answering the following questions: • What is the main topic of the article? • What was/were the main issue(s) the author said they want to discuss? • Why did the author claim it was important? • How does the work build on other's work, in the author's opinion? • What simplifying assumptions does the author claim to be making? • What did the author do? • How did the author claim they were going to evaluate their work and compare it to others?	5th week	**8%** (the table given should indicate your understanding of the paper and the evaluation is based on your conclusions about each paper)

	• What did the author say were the limitations of their research? • What did the author say were the important directions for future research? • Conclude with limitations/issues not addressed by the paper (from the perspective of your survey)		
Reading and notes for next5 papers	Repeat Reading Paper Process	6th week	**8%** (the table given should indicate your
Draft outline 1 and Linking papers	Prepare a draft Outline, with survey goals, along with a classification / categorization Diagram	8th week	**8%** (this component will be evaluated based on the linking and classification among the papers)
Abstract	Prepare a draft abstract and give a Presentation	9th week	**6%** (Clarity, purpose and conclusion) **6%** Presentation & Viva Voce
Introduction Background	Write an introduction and background Sections	10th week	**5%** (clarity)
Sections of the paper	Write the sections of the paper chosen based on the classification / categorization diagram in keeping with the goals of your survey	11thweek	**10%** (this component will be evaluated based on the linking and classification among the papers)
Your conclusions	Write conclusions and future work	12th week	**5%** (conclusions– clarity and your ideas)
Final Draft	Complete the final draft of the paper prepared	13th week	**10%** (formatting, English, Clarity and linking) **4%** Plagiarism

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			Check Report
Seminar	A brief 15 slides on the paper prepared	14^{th}& 15^{th} week	**10%** (based on presentation and Viva-voce)

Course Designer(s)

Mr.S.Saravanan – saravanan.s@ksrct.ac.in

K.S. RANGASAMY COLLEGE OF TECHNOLOGY, TIRUCHENGODE - 637215
(An Autonomous Institution affiliated to Anna University)

M.E. / M.Tech. Degree Programme

SCHEME OF EXAMINATIONS
(For the candidates admitted in 2025-2026)

THIRD SEMESTER

S.No	Course Code	Name of the Course	Duration of Internal Exam	Weightage of Marks			Minimum Marks for Pass in End Semester Exam	
				Continuous Assessment *	End Semester Exam **	Max. Marks	End Semester Exam	Total
THEORY								
1.	70 PVL 301	Electronic Packaging	2	40	60	100	45	100
2.	70 PVL E4*	Professional Elective IV	2	40	60	100	45	100
THEORY CUM PRACTICAL								
3.	70 PVL E5*	Professional Elective V	2	50	50	100	45	100
PRACTICAL								
4.	70 PVL 3P1	Project Work-Phase I	3	100	00	100	-	100

* CA evaluation pattern will differ from course to course and for different tests. This will have to be declared in advance to students. The department will put a process in place to ensure that the actual test paper follow the declared pattern.

** End semester Examination will be conducted for maximum marks of 100 and subsequently be reduced to 60 marks for theory End Semester Examination, 50 marks for theory cum practical End Semester Examination and 40 marks for practical End semester Examination.

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70 PVL 301	Electronic Packaging	Category	L	T	P	Credit
		PC	3	0	0	3

Objectives

- To understand the fundamental concepts of electronic systems packaging
- To understand the packaging optimize materials for electronic systems
- To explore the knowledge of CAD for printed circuit board
- To illustrate the concepts of Surface Mount Technology and Thermal Management
- To study about the Embedded passive Technology

Pre-requisites

- Electronic Circuits and Embedded Systems

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Explain the electronic systems packaging	Understand
CO2	Describe the packaging optimize materials	Analyse
CO3	Design CAD for printed circuit board	Understand
CO4	Describe Surface Mount Technology and Thermal Management	Understand
CO5	Illustrate the Embedded passive Technology	Understand

Mapping with Programme Outcomes

COs	POs					
	1	2	3	4	5	6
CO1	3	3	3	2	2	3
CO2	3	3	3	-	2	3
CO3	3	3	3	-	2	3
CO4	3	3	3	2	2	3
CO5	3	3	3	-	2	3
3 - Strong; 2 - Medium; 1 - Some						

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	10	20	30
Understand	20	40	10
Apply	20	-	30
Analyse	10	-	30
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

Passed in BoS Meeting held on 13/06/2025
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Syllabus

K.S.Rangasamy College of Technology – Autonomous R2025

M.E-VLSI Design

70 PVL 301 – Electronic Packaging

Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
III	3	0	0	45	3	40	60	100

Electronic Systems Packaging * Definition of a System and History of Semiconductors, Products and Levels of Packaging, Packaging Aspects of Handheld Products, Definition of PWB, Basics of Semiconductor and Process Flowchart, Wafer Fabrication, Inspection and Testing, Wafer Packaging; Packaging Evolution; Chip Connection Choices, Wire Bonding, TAB and Flip Chip.	[9]
Semiconductor Packages * Single Chip Packages or Modules (SCM), Commonly Used Packages and Advanced Packages; Materials in Packages; Thermal Mismatch in Packages; Multichip Modules (MCM)-Types; System-in-Package (SIP); Packaging Roadmaps; Hybrid Circuits; Electrical Design Considerations In Systems Packaging, Resistive, Capacitive and Inductive Parasitic, Layout Guidelines and the Reflection Problem, Interconnection.	[9]
CAD for Printed Wiring Boards* Benefits From CAD; Introduction to DFM, DFR & DFT, Components of a CAD Package and Its Highlights - Circuit Design - Design for Reliability, Printed Wiring Board Technologies: Board - Level Packaging Aspects, Review of CAD Output Files for PCB Fabrication; Photo Plotting and Mask Generation, Process Flow-Chart; Vias; PWB Substrates; Surface Preparation, Photoresist and Application Methods; UV Exposure and Developing; Printing Technologies for PWBs, PWB Etching; Resist Stripping; Screen Printing Technology, Through-Hole Manufacture Process Steps; Panel and Pattern Plating Methods, Solder Mask for PWBs and Multilayer PWBs.	[9]
Surface Mount Technology and Thermal Considerations* SMD Benefits; Design Issues, Reflow and Wave Soldering Methods to Attach SMDs, Solders; Wetting of Solders; Flux and Its Properties; Defects In Wave Soldering, Vapour Phase Soldering, BGA Soldering and Desoldering/Repair; SMT Failures, SMT Failure Library and Tin Whisker, Tin-Lead and Lead-Free Solders; Phase Diagrams; Thermal Profiles for Reflow Soldering; Lead Free alloys, Lead-Free Solder Considerations; Green Electronics; Rohs Compliance and E-Waste Recycling, Issues, Thermal Design Considerations in Systems Packaging.	[9]
Embedded Passives Technology* Introduction to Embedded Passives; Need for Embedded Passives; Design Library; Embedded Resistor Processes, Embedded Capacitors; Processes for Embedding Capacitors; Case Study: Implementation of Embedded Passives Technology in Mobile Devices	[9]
Total Hours	45

Text Book(s):	
1.	Rao R. Tummala, “Fundamentals of Microsystems Packaging”, McGraw Hill, NY, 2001.
2.	R.G. Kaduskar and V.B.Baru, Electronic Product design, Wiley India, 2011
Reference(s):	
1.	Tummala, Rao R, Microelectronics packaging handbook, McGraw Hill, 2008.
2.	William D. Brown, “Advanced Electronic Packaging”, IEEE Press, 1999.
3.	R.S.Khandpur, Printed Circuit Board, Tata McGraw Hill, 2005

*SDG-Industry Innovation and Infrastructure

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Course Contents and Lecture Schedule		
S. No.	**Topics**	**No. of hours**
1	**Overview of Electronic Systems Packaging**	
1.1	Definition of a system and history of semiconductors	1
1.2	Products and levels of packaging	1
1.3	Packaging aspects of handheld products	1
1.4	Definition of PWB	1
1.5	Basics of Semiconductor and Process flowchart	1
1.6	Wafer fabrication, inspection and testing	1
1.7	Wafer packaging; Packaging evolution	1
1.8	Chip connection choices	1
1.9	Wire bonding, TAB and flip chip	1
2	**Semiconductor Packages**	
2.1	Single chip packages or modules (SCM)	1
2.2	Materials in packages; Thermal mismatch in packages	1
2.3	Commonly used packages and advanced packages	1
2.4	Multichip modules (MCM)-types	1
2.5	System-in-package (SIP)	1
2.6	Packaging roadmaps Hybrid circuits	1
2.7	Electrical Design considerations in systems packaging	1
2.8	Resistive, Capacitive and Inductive Parasitics	1
2.9	Layout guidelines and the Reflection problem, Interconnection	1
3	**CAD for Printed Wiring Boards**	
3.1	Benefits from CAD; Introduction to DFM, DFR & DFT	1
3.2	Components of a CAD package and its highlights, Beginning a circuit design with schematic work and component layout	1
3.3	DFM check, list and design rules	1
3.4	Design for Reliability, Printed Wiring Board Technologies: Board-level packaging aspects, Review of CAD output files for PCB fabrication	1
3.5	Photo plotting and mask generation, Process flow-chart; Vias	1
3.6	PWB substrates; Surface preparation, Photoresist and application methods	1
3.7	UV exposure and developing; Printing technologies for PWBs, PWB etching; PWB etching, Resist stripping	1
3.8	Screen printing technology, through-hole manufacture process steps; Panel and pattern plating methods, Solder mask for PWBs; Multilayer PWBs	1
3.9	Introduction to, microvias, Microvia technology and Sequ	
4	**Surface Mount Technology and Thermal Considerations**	
4.1	SMD benefits; Design issues; Introduction to soldering	1
4.2	Reflow and Wave Soldering methods to attach SMDs	1
4.3	Solders; Wetting of solders; Flux and its properties	1
4.4	Defects in wave soldering, Vapour phase soldering	1
4.5	BGA soldering and Desoldering/Repair; SMT failures	1
4.6	SMT failure library and Tin Whisker, Tin-lead and lead-free solders	1
4.7	Phase diagrams; Thermal profiles for reflow soldering; Lead freevAlloys	1

4.8	Lead-free solder considerations; Green electronics; RoHS	1
4.9	compliance and e-waste recycling, Issues, Thermal Design considerations in systems packaging	
5	**Embedded Passives Technology**	
5.1	Introduction to embedded passives	1
5.2	Need for embedded passives	1
5.3	Design Library	1
5.4	Embedded resistor processes	1
5.5	Embedded capacitors	1
5.6	Processes for embedding capacitors	2
5.7	Case study examples	2

Course Designer(s)

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70 PVL E41	DSP Structures for VLSI	Category	L	T	P	Credit
		PE	3	0	0	3

Objectives

- To understand the fundamentals of DSP
- To learn various DSP structures and their implementation.
- To know designing constraints of various filters
- Design and optimize VLSI architectures for basic DSP algorithms
- To enable students to design VLSI system with high speed and low power.

Pre-requisites

- Digital Signal Processing

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Acquire knowledge about fundamentals of DSP processors.	Apply
CO2	Improve the overall performance of DSP system through various transformation and optimization techniques.	Apply
CO3	Understand the need of different types of instructions for DSP.	Apply
CO4	Optimize design in terms of computation complexity and speed.	Apply
CO5	Understand clock based issues and design asynchronous and wave pipelined systems.	Understand

Mapping with Programme Outcomes

COs	POs					
	1	2	3	4	5	6
CO1	3	3	3	3	-	3
CO2	3	3	3	3	-	3
CO3	3	3	3	3	-	3
CO4	3	3	3	3	-	3
CO5	3	3	3	3	-	3
3 - Strong; 2 - Medium; 1 - Some						

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	10	10	10
Understand	10	20	30
Apply	40	30	60
Analyse	-	-	-
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

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K.S.Rangasamy College of Technology

Syllabus

K.S.Rangasamy College of Technology – Autonomous R2025

M.E-VLSI Design

70 PVL E41 – DSP Structures for VLSI

Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
III	3	0	0	45	3	40	60	100

Introduction to Digital Signal Processing Linear System Theory- Convolution- Correlation - DFT- FFT- Basic Concepts in FIR Filters and IIR Filters- Filter Realizations. Representations of DSP Algorithms- Block Diagram-SFG-DFG.	[9]
Iteration Bound, Pipelining and Parallel Processing of Fir Filter Data-flow Graph Representations- Loop Bound and Iteration Bound Algorithms for Computing Iteration Bound-LPM Algorithm. Pipelining and Parallel Processing: Pipelining of FIR Digital Filters Parallel Processing, Pipelining and Parallel Processing for Low Power.	[9]
Retiming, Unfolding and Folding Retiming: Definitions, Properties and Problems- Solving Systems of Inequalities. Properties of Unfolding, Critical Path, Unfolding and Retiming, Applications of Unfolding, Folding Transformation Register Minimization Techniques, Register Minimization in Folded Architecture- Folding of Multirate System.	[9]
Fast Convolution Cook-Toom Algorithm- Modified Cook - Toom Algorithm. Design of Fast Convolution Algorithm by Inspection - Winograd Algorithm- Modified Winograd Algorithm.	[9]
Arithmetic Strength Reduction in Filters Parallel Fir Filters-Fast Fir Algorithms-Two Parallel and Three Parallel. Parallel Architectures for Rank Order Filters -Odd-Even, Merge-Sort Architecture-Rank Order Filter Architecture-Parallel Rank Order Filters-Running Order, Merge Order Sorter, Low Power Rank Order Filter.	[9]
Total Hours	**45**

Reference(s):

1. K.K Parhi: "VLSI Digital Signal Processing", John-Wiley, 2nd Edition, Reprint, 2008.
2. John G.Proakis, Dimitris G.Manolakis, "Digital Signal Processing", Prentice Hall of India, 1st Edition, 2009.

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Approved in Academic Council Meeting held on 19/07/2025

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Course Contents and Lecture Schedule		
S. No.	**Topics**	**No. of hours**
1.0	**Introduction to Digital Signal Processing**	
1.1	Linear System Theory, Convolution and Correlation	1
1.2	DFT & FFT	2
1.3	Basic Concepts in FIR Filters and IIR Filters	2
1.4	Filter Realizations	2
1.5	Representations of DSP Algorithms- Block Diagram, SFG, DFG.	2
2.0	**Iteration Bound, Pipelining and Parallel Processing of Fir Filter**	
2.1	Data-Flow Graph Representations	1
2.2	Loop Bound and Iteration Bound Algorithms for Computing Iteration Bound	2
2.3	LPM Algorithm	2
2.4	Ppipelining of FIR Digital Filters Parallel Processing,	2
2.5	Pipelining and Parallel Processing for Low Power	2
3.0	**Retiming, Unfolding and Folding**	
3.1	Retiming: Definitions, Properties and Problem Solving Systems of Inequalities	2
3.2	Properties of Unfolding, Critical Path, Unfolding and Retiming	2
3.3	Applications of Unfolding	1
3.4	Folding Transformation Register Minimization Techniques	2
3.5	Register Minimization in Folded Architecture	1
3.6	Folding of Multirate System	1
4.0	**Fast Convolution**	
4.1	Cook-Toom Algorithm	2
4.2	Modified Cook-Toom Algorithm	2
4.3	Design of Fast Convolution Algorithm	2
4.4	By Inspection - Winograd Algorithm	2
4.5	Modified Winograd Algorithm	1
5.0	**Arithmetic Strength Reduction in Filters**	
5.1	Parallel FIR Filters	1
5.2	Fast FIR Algorithms-Two Parallel and Three Parallel	2
5.3	Parallel Architectures for Rank Order Filters -Odd-Even	2
5.4	Merge-Sort Architecture-Rank Order Filter Architecture	1
5.5	Parallel Rank Order Filters	1
5.6	Running Order Merge Order Sorter	1
5.7	Low Power Rank Order Filter	1

Course Designer(s)

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70 PVL E42	Applied Medical Image Processing	Category	L	T	P	Credit
		PE	3	0	0	3

Objectives

- To introduce the fundamentals of image processing techniques
- To apply the enhancement techniques and analyse the image
- To learn about medical image representation
- To analyse the quality of medical image and do classification
- To study about image registrations and visualizations

Pre-requisites

- Nil

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Explain the fundamentals of image processing	Understand
CO2	Analyze Morphology, enhancement techniques and implement these in images	Apply
CO3	Understand the representation of medical images	Apply
CO4	Analyze medical images of numerous modalities such as PET, MRI, CT, or microscopy	Apply
CO5	Study image registrations and visualization	Apply

Mapping with Programme Outcomes

COs	POs					
	1	2	3	4	5	6
CO1	3	-	2	-	2	-
CO2	3	-	3	2	3	3
CO3	3	-	3	2	3	3
CO4	3	-	3	2	3	3
CO5	3	-	3	2	3	-
3 - Strong; 2 - Medium; 1 - Some						

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	10	10	30
Understand	30	30	30
Apply	20	20	30
Analyse	-	-	10
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

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Syllabus

K.S.Rangasamy College of Technology – Autonomous R2025								
M.E-VLSI Design								
70 PVL E42- Applied Medical Image Processing								
Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
III	3	0	0	45	3	40	60	100

Image Fundamentals Image Perception, MTF of the Visual System, Image Fidelity Criteria, Image Model, Image Sampling and Quantization — Two-Dimensional Sampling Theory, Image Quantization, Optimum Mean Square Quantizer, Image Transforms — DFT, DCT, KLT, SVD.	[9]
Image Enhancement and Restoration Histogram Equalization and Specification Techniques, Noise Distributions, Spatial Averaging, Directional Smoothing, Median, Geometric Mean, Harmonic Mean, Contra Harmonic Mean Filters, Homomorphic Filtering, Color Image Enhancement. Image Restoration - Degradation Model, Unconstrained and Constrained Restoration, Inverse Filtering- Wiener Filtering.	[9]
Medical Image Representation Pixels and Voxels – Algebraic Image Operations - Gray Scale and Color Representation- Depth-Color and Look Up Tables - Image File Formats- Dicom- Other Formats- Analyze 7.5, Nifti and Interfile, Image Quality and the Signal to Noise Ratio.	[9]
Medical Image Analysis and Classification Image Segmentation- Pixel Based, Edge Based, Region Based Segmentation. Image Representation and Analysis, Feature Extraction and Representation, Statistical, Shape, Texture, Feature and Image Classification — Statistical, Rule Based, Neural Network Approaches.	[9]
Image Registrations and Visualization Rigid Body Visualization, Principal Axis Registration, Interactive Principal Axis Registration, Feature Based Registration, Elastic Deformation Based Registration, Image Visualization — 2D Display Methods, 3D Display Methods, Virtual Reality Based Interactive Visualization.	[9]
Total Hours	**45**

Text book(s):

1	Atam P.Dhawan, "Medical Image Analysis", Wiley Interscience Publication, NJ, USA, 2nd Edition 2011.
2	Anil. K. Jain, "Fundamentals of Digital Image Processing", Pearson education, Indian Reprint 2003.

Reference(s):

1.	John L.Semmlow,"Biosignal and Biomedical Image Processing Matlab Based applications", Marcel Dekker Inc.,New York,2004
2.	Kavyan Najarian and Robert Splerstor, "Biomedical signals and Image processing", CRC – Taylor and Francis, New York, 2006
3.	R.C.Gonzalez and R.E.Woods, "Digital Image Processing", 2nd Edition, Pearson Education, 2002.

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Approved in Academic Council Meeting held on 19/07/2025

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Course Contents and Lecture Schedule		
S. No.	**Topics**	**No. of hours**
1.0	**Image Fundamentals**	
1.1	Image Perception	1
1.2	MTF of the Visual System	1
1.3	Image Fidelity Criteria	1
1.4	Image Model	1
1.5	Image Sampling and Quantization	1
1.6	Two-Dimensional Sampling Theory	1
1.7	Image Quantization, Optimum Mean Square Quantizer	1
1.8	Image Transforms – DFT, DCT	1
1.9	KLT, SVD	1
2.0	**Image Enhancement and Restoration**	
2.1	Histogram Equalization and Specification Techniques	1
2.2	Noise Distributions,	1
2.3	Spatial Averaging, Directional Smoothing,	1
2.4	Median, Geometric Mean, Harmonic Mean,	1
2.5	Contra Harmonic Mean Filters, Homomorphic Filtering	1
2.6	Color Image Enhancement	1
2.7	Image Restoration - Degradation Model,	1
2.8	Unconstrained and Constrained Restoration	1
2.9	Inverse Filtering- Wiener Filtering	1
3.0	**Medical Image Representation**	
3.1	Pixels and Voxels – Algebraic Image	2
3.2	Operations - Gray Scale and Color Representation	1
3.3	Depth-Color and Look Up Tables	1
3.4	Image File Formats	1
3.5	DICOM- Other Formats	1
3.6	Analyze 7.5 Nifti and Interfile	2
3.7	Image Quality and the Signal to Noise Ratio	1
4.0	**Medical Image Analysis and Classification**	
4.1	Image Segmentation	1
4.2	Pixel Based, Edge Based, Region Based Segmentation	2
4.3	Image Representation and Analysis	1
4.4	Feature Extraction and Representation	2
4.5	Statistical, Shape, Texture, Feature	1
4.6	Image Classification	1
4.7	Neural Network Approaches	1
5.0	**Image Registrations and Visualization**	
5.1	Rigid Body Visualization	2
5.2	Principal Axis Registration	1
5.3	Interactive Principal Axis Registration	1
5.4	Feature Based Registration	1
5.5	Elastic Deformation Based Registration	1

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5.6	Image Visualization – 2D Display Methods, 3D Display Methods	1

5.7	Virtual Reality Based Interactive Visualization	2

Course Designer(s)

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70 PVL E43	Data Science and Engineering	Category	L	T	P	Credit
		PE	3	0	0	3

Objectives

- To understand the concepts and technologies in data science
- To explore the concepts in statistical inference and exploratory data analysis
- To understand the basic machine learning algorithms
- To explore the effective visualization of given data using visualization tools
- To implement the data science applications

Pre-requisites

- Nil

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Understand the basics of Data Sciences	Understand
CO2	Explain mathematical foundations needed for data Science and perform Exploratory Data Analysis.	Understand
CO3	Implement models such as k-nearest Neighbors, Naive Bayes, linear and logistic Regression, decision trees, neural networks and clustering.	Apply
CO4	Create effective visualization of given data	Apply
CO5	Build data science applications	Apply

Mapping with Programme Outcomes

COs	POs					
	1	2	3	4	5	6
CO1	3	3	3	-	3	-
CO2	3	3	3	-	3	-
CO3	3	3	3	-	3	-
CO4	3	3	3	-	3	-
CO5	3	3	3	-	3	-
3 - Strong; 2 - Medium; 1 - Some						

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	30	10	20
Understand	30	10	20
Apply	-	40	60
Analyse	-	-	-
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

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Syllabus

K.S.Rangasamy College of Technology – Autonomous R2025

M.E-VLSI Design

70 PVL E43-Data Science and Engineering

Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
III	3	0	0	45	3	40	60	100

Introduction to core concepts and technologies Introduction, Terminology, Data-Properties of Data, Types of data, Why Data Science? Computer Science, Data Science, and Real Science, data science process, Data Acquisition and Data Science Life Cycle, Ethics in Data Science, data science toolkit, Example applications. Data wrangling: Sources of data, Data collection and API, Working with data: Reading Files, Cleaning Data.	[9]
Statistical Inference, Exploratory Data Analysis Statistical thinking in Data Science, Statistical Inference, Statistical Analysis, Modeling, Exploratory Data Analysis: Philosophy of Exploratory Data Analysis, Data visualization, Missing value analysis, The correction matrix, Outlier detection analysis	[9]
Basic Machine Learning Algorithms Brief introduction, Linear / Polynomial Regression, Logistic Regression, Classification, Regularization, Support vector machines, Extreme learning machines, Naive Bayes, Cross Validation, Label Encoding, Random Forests, Decision Trees, Clustering, Dimensionality reduction, Manifold learning, 2D/3D Convolution, Introduction to Neural Networks, Evaluation Metrics.	[9]
Data visualization Introduction, Types of data visualization, Data Visualization - Basic principles, ideas and tools for basic data visualization tools (plots, graphs and summary statistics)- various visualization techniques used in Data Science. Data visualization Tool: Working with Tableau, Creating charts, Mapping data in Tableau. create your own visualization of a complex dataset	[9]
Applications of Data Science Case Studies of Data Science Application, Recommender Systems on Real World Data Sets, Weather forecasting, Stock market prediction, Object recognition, Matching Skills to Job.	[9]
Total Hours	**45**

Text book(s):

1	Cathy O'Neil, Rachel Schutt, "Doing Data Science, Straight Talk from The Frontline", O'Reilly, 2015.
2	Joel Grus, "Data Science from Scratch: First Principles with Python", O'Reilly Media.

Reference(s):

1.	Jure Leskovek, Anand Rajaraman, Jeffrey Ullman, Mining of Massive Datasets. v2.1, Cambridge University Press, 2014.
2.	Aurélien Géron, "Hands-On Machine Learning with Scikit-Learn and Tensor Flow: Concepts, Tools, and Techniques to Build Intelligent Systems", 1st Edition, O'Reilly Media
3.	Jiawei Han and Jian Pei, "Data Mining Concepts and Techniques", 3rd Edition, Morgan Kaufmann Publishers
4.	Jain V.K., "Data Sciences", Khanna Publishing House, Delhi.

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Course Contents and Lecture Schedule		
S. No.	**Topics**	**No. of hours**
1.0	**Introduction to Core Concepts and Technologies**	
1.1	Introduction, Terminology, Data-Properties of Data, Types of Data	1
1.2	Why Data Science? Computer Science, Data Science, and Real Science, Data Science Process	1
1.3	Data Acquisition and Data Science Life Cycle	1
1.4	Ethics in Data Science, Data Science Toolkit, Example Applications.	2
1.5	Data Wrangling: Sources of Data	1
1.6	Data Collection and API	1
1.7	Working with Data: Reading Files, Cleaning Data.	1
2.0	**Statistical Inference, Exploratory Data Analysis:**	
2.1	Statistical Thinking in Data Science	1
2.2	Statistical Inference, Statistical Analysis, Modeling	2
2.3	Exploratory Data Analysis & Data Visualization	2
2.4	Missing Value Analysis	2
2.5	The Correction Matrix, Outlier Detection Analysis	2
3.0	**Basic Machine Learning Algorithms**	
3.1	Brief Introduction, Linear / Polynomial Regression, Logistic Regression	1
3.2	Classification, Regularization	1
3.3	Support Vector Machines, Extreme Learning Machines, Naive Bayes	2
3.4	Cross Validation, Label Encoding	1
3.5	Random Forests, Decision Trees	1
3.6	Clustering, Dimensionality Reduction	1
3.7	Manifold Learning, 2D/3D Convolution	1
3.8	Introduction to Neural Networks	1
4.0	**Data Visualization**	
4.1	Introduction, Types of Data Visualization, Data Visualization	1
4.2	Basic Principles, Ideas and Tools for Basic Data Visualization Tools (Plots, Graphs and Summary Statistics)-	2
4.3	Data Extraction and Filtering, Data Visualization Principles.	2
4.4	Data Visualization Tool: Random Sample Generation Using Tableau, Remote Database Connectivity	2
4.5	Creating Charts	1
4.6	Mapping Data in Tableau	1
4.7	Create Your Own Visualization of a Complex Dataset	1
5.0	**Applications of Data Science**	
5.1	Case Studies of Data Science Application	2
5.2	Recommended Systems on Real World Data Sets	1
5.3	Weather Forecasting	1
5.4	Stock Market Prediction	2
5.5	Object Recognition	1
5.6	Matching Skills to Job	1

Course Designer(s)

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70 PVL E44	Data Converters IC Design	Category	L	T	P	Credit
		PE	3	0	0	3

Objectives

- To Understand the Fundamentals of Data Conversion.
- To Design and Analyze Switched-Capacitor Circuits and Comparators.
- To Comprehend Nyquist-Rate DAC Architectures.
- To Evaluate Pipeline and Other ADC Architectures
- To Explore Sigma-Delta Conversion Techniques

Pre-requisites

- Nil

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Explain the design calculations for developing the various blocks associated with a typical CMOS AD or DA converter.	Understand
CO2	Design and implement circuits using switched capacitor concepts	Apply
CO3	Analyze and design D/A converters	Analyse
CO4	Design different types of A/Ds	Apply
CO5	Analyze and design sigma delta converters	Apply

Mapping with Programme Outcomes

COs	POs					
	1	2	3	4	5	6
CO1	3	3			2	3
CO2	3	3	3	3	2	3
CO3	3	3		3	2	3
CO4	3	3			2	3
CO5	3	3	3	3	2	3
3 - Strong; 2 - Medium; 1 - Some						

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	14	6	10
Understand	14	6	10
Apply	22	38	70
Analyse	10	10	10
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

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Syllabus

K.S.Rangasamy College of Technology – Autonomous R2025

M.E-VLSI Design

70 PVL E44 – Data Converters IC Design

Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
III	3	0	0	45	3	40	60	100

Introduction & characteristics of AD/DA converter characteristics Evolution, types and applications of AD/DA characteristics, issues in sampling, quantization and reconstruction, oversampling and antialiasing filters.	[9]
Switch capacitor circuits and comparators Switched-capacitor amplifiers, switched capacitor integrator, switched capacitor common mode feedback. Single stage amplifier as comparator, cascaded amplifier stages as comparator, latched comparators. offset cancellation, Op Amp offset cancellation, Calibration techniques	[9]
NYQUIST rate D/A converters Current Steering DACs, capacitive DACs, Binary weighted versus thermometer DACs, issues in current element matching, clock feed through, zero order hold circuits, DNL, INL and other performance metrics of ADCs and DACs	[9]
Pipeline and other ADCs Performance metrics, Flash architecture, Pipelined Architecture, Successive approximation architecture, Time interleaved architecture.	[9]
SIGMA DELTA converters STF, NTF, first order and second order sigma delta modulator characteristics, Estimating the maximum stable amplitude, CTDSMs, Opamp nonlinearities	[9]
Total Hours: 45 + 15(Tutorial)	**60**

Text Book(s):

1.	Shanthi Pavan, Richard Schreier, Gabor C. Temes , "Understanding Delta-Sigma Data Converters", 2nd Edition, Willey-IEEE Press, 2017
2.	Rudy van de Plassche, "CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters", Boston, 2nd Edition, Kluwer Acedamic Publishers, December 2010

Reference(s):

1.	J. G. Proakis, D. G. Manolakis, "Digital Signal Processing Principles, Algorithms and Applications", 4th Edition, Prentice Hall January 2014

*SDG 4: Quality education.

**SDG 9: Promote inclusive and sustainable industrialization

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Course Contents and Lecture Schedule

S. No.	Topics	No. of hours
1.0	**Introduction& Characteristics of AD/DA converter characteristics**	
1.1	Evolution	1
1.2	types and applications of AD/DA characteristics	2
1.3	Issues in sampling	2
1.4	quantization and reconstruction	2
1.5	oversampling and antialiasing filters	2
2.0	**Switch capacitor circuits and comparators**	
2.1	Switched-capacitor amplifiers	1
2.2	switched capacitor integrator	1
2.3	switched capacitor common mode feedback	1
2.4	Single stage amplifier as comparator	1
2.5	latched comparators	1
2.6	offset cancellation	1
2.7	Op Amp offset cancellation	1
2.9	, Calibration techniques	1
3.0	**NYQUIST rate d/a converters**	
3.1	Current Steering DACs	1
3.2	capacitive DACs	1
3.3	Binary weighted versus thermometer DACs	1
3.4	issues in current element matching	1
3.5	clock feed through	1
3.6	zero order hold circuits	1
3.7	DNL	1
3.8	INL and other performance metrics of ADCs and DACs	2
4.0	**Pipeline and other ADCs**	
4.1	Performance metrics	1
4.2	Flash architecture	2
4.3	Pipelined Architecture	2
4.4	Time interleaved architecture	2
4.5	Successive approximation architecture	2
5.0	**SIGMA DELTA converters**	
5.1	STF	2
5.2	NTF	1
5.3	first order and second order sigma delta modulator characteristics	2
5.4	Estimating the maximum stable amplitude	2
5.5	CTDSMs	1
5.6	Opamp nonlinearities	2

Course Designer(s)

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70 PVL E45	Mixed Signal VLSI Design	Category	L	T	P	Credit
		PE	3	0	0	3

Objectives

- To know the types of filters for VLSI circuits.
- To explain the different techniques of ADC for mixed signal circuits.
- To introduce the different techniques of DAC for mixed signal circuits.
- To learn about sigma delta converters for mixed signal circuits.
- To learn the design methodologies and EDA tools for mixed signal VLSI circuits

Pre-requisites

- Nil

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Describe the concept of different filter for VLSI circuit design.	Apply
CO2	Explain the function of continuous time filter in MOS technology for mixed signal circuits.	Apply
CO3	Apply DAC and ADC techniques for data conversions using CMOS Technologies.	Apply
CO4	Illustrates the concept of sigma delta converter method for VLSI Circuits.	Apply
CO5	Design a complete mixed signal system using EDA tools.	Analyze

Mapping with Programme Outcomes

COs	POs					
	1	2	3	4	5	6
CO1	3	3	2	3	-	3
CO2	3	3	3	3	-	3
CO3	3	3	3	3	3	3
CO4	3	-	2	3	2	3
CO5	3	3	3	3	3	3
3 - Strong; 2 - Medium; 1 - Some						

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	12	10	20
Understand	28	30	50
Apply	20	10	20
Analyse	-	10	10
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

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K.S.Rangasamy College of Technology – Autonomous R2025

M.E-VLSI Design

70 PVL E45- Mixed Signal VLSI Design

Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
III	3	0	0	45	3	40	60	100

Active Filters & Switched Capacitor Filters Switched Capacitor (SC) Circuits: Parasitic Insensitive Switched Capacitor Amplifiers- Insensitive Integrators - Signal Flow - Graph Analysis - Switched capacitor filters and Resistors - Comparators - CMOS, BICMOS Sample-and- Holds - Linearity, Fully Differential Switched Capacitor Circuits - Noise in Switched Capacitor Circuits - Integrator- Biquadratic SC Filter- SC N-Path Filters.	[9]
Continuous Time Filters Introduction to Gm - C Filters - Bipolar Transconductors - CMOS Transconductors using Triode Transistors, Active Transistors - BiCMOS transconductors - MOSFET C Filters - Tuning Circuitry - Dynamic Range Performance -Elementary transconductor Building Block- First and Second Order Filters.	[9]
Digital to Analog & Analog to Digital Converters Types of DAC's: Current Switched, Resistive, Current Cell Design in Current Steering DAC, Hybrid Converters, Segmented Converters DAC's - Techniques for Improving Linearity - Analog to Digital Converters: Quantization Errors - non-Idealities - Types of ADC's: Flash, folding ADC's, Multiple-Bit Pipeline ADCs and SAR ADC, Time - Interleaved A/D Converters	[9]
Sigma Delta Converters Over Sampled Converters - Over Sampling without Noise & with Noise - implementation Imperfections - First Order Modulator - Decimation Filters - Second Order Modulator - Sigma Delta DAC & ADC's - Discrete Delta Sigma Modulator - Based ADC using MATLAB	[9]
Analog and Mixed Signal Extensions to HDL Language Design Objectives - Theory of Differential Algebraic Equations - the 1076 .1 Language - Tolerance Groups - Conservative Systems - Time and the Simulation Cycle - A/D and D/A Interaction - Quiescent Point - Frequency Domain Modeling and Examples-Analog Extensions to Verilog: Mixed Signal HDL Design Flow- data types - Expressions - Signals- Analog behavior - Hierarchical Structures - Mixed Signal Interaction	[9]
Total Hours	**45**

Text book(s):

1.	David A Johns and Ken Martin, "Analog Integrated Circuit Design", John Wiley and Sons, 2016.
2.	Rudy van de Plassche, "Integrated Analog-to-Digital and Digital-to-Analog Converters", Kluwer, 2014.

Reference(s):

1.	B. Razavi, "Design of Analog CMOS Integrated Circuits", Tata McGraw Hill, 2002, Reprint 2015.
2.	Michael D.Ciletti, "Advanced Digital Design with the Verilog HDL", 2nd Edition, Pearson Education, 2011.
3.	Antoniou, "Digital Filters Analysis and Design", Tata McGraw Hill, 2010.
4.	Yuan Taur and Tak H.Ning, "Fundamentals of Modern VLSI Devices", Cambridge University Press, 2016.

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Course Contents and Lecture Schedule

S. No.	Topics	No. of hours
1.0	**Introduction to Active Filters & Switched Capacitor Filters**	
1.1	Switched Capacitor (SC) Circuits: Parasitic Insensitive Switched Capacitor Amplifiers	2
1.2	Insensitive Integrators - Signal Flow - Graph Analysis -Switched Capacitor Filters and Resistors	2
1.3	Comparators - CMOS, BICMOS Sample-and-Holds	2
1.4	Linearity, Fully Differential Switched Capacitor Circuits - Noise in Switched Capacitor Circuits	1
1.5	Integrator- Biquadratic SC Filter	1
1.6	SC N-Path Filters.	1
2.0	**Continuous Time Filters**	
2.1	Introduction to Gm - C Filters	1
2.2	Bipolar Transconductors	1
2.3	CMOS Transconductors using Triode Transistors, Active Transistors	2
2.4	BiCMOS transconductors	1
2.5	MOSFET C Filters - Tuning Circuitry	1
2.6	Dynamic Range Performance - Elementary Transconductor Building Block	2
2.7	First and Second Order Filters	1
3.0	**Digital to Analog & Analog to Digital Converters**	
3.1	Types of DAC's: Current Switched, Resistive, Current Cell Design in Current Steering DAC	2
3.2	Hybrid Converters, Segmented Converters DAC's	2
3.3	Techniques for Improving Linearity - Analog to Digital Converters	1
3.4	Quantization Errors - Non-Idealities - types of ADC's: Flash, Folding ADC's	2
3.5	Multiple-Bit Pipeline ADCs and SAR ADC, Time-Interleaved A/D Converters	2
4.0	**Sigma Delta Converters**	
4.1	Over Sampled Converters - Over Sampling without Noise & with Noise	2
4.2	Implementation Imperfections - First Order Modulator	2
4.3	Decimation Filters - Second Order Modulator	1
4.4	Sigma Delta DAC & ADC's	2
4.5	Discrete Delta Sigma Modulator-Based ADC using MATLAB	1
5.0	**Analog and Mixed Signal Extensions to HDL**	
5.1	Introduction - Language Design Objectives - Theory of Differential Algebraic Equations	1
5.2	The 1076 .1 Language - Tolerance groups	1
5.3	Tolerance Groups - Conservative Systems - Time and the Simulation Cycle	2
5.4	A/D and D/A Interaction - Quiescent Point - Frequency Domain Modeling and Examples	2
5.5	Analog Extensions to Verilog: Mixed Signal HDL Design Flow- Data Types - Expressions	2
5.6	Signals- Analog Behavior - Hierarchical Structures –Mixed Signal interaction	2

Course Designer(s)

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70 PVL E51	System Verilog	Category	L	T	P	Credit
		PE	3	0	2	4

Objectives

- To understand the end-to-end functional verification flow, including directed vs. constrained-random testing.
- To apply layered test bench architecture by constructing drivers, monitors, scoreboards, and agents in System Verilog.
- To remember and use key language constructs (data types, procedural blocks, simple assertions) to model test bench behavior.
- To create modular, object-oriented verification components using classes, inheritance, and encapsulation.
- To analyse functional coverage data (cover groups, cover points, crosses) to measure and drive verification completeness.

Pre-requisites

- Verilog HDL

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Apply both directed and constrained-random stimulus generation within a layered testbench.	Apply
CO2	Implement System Verilog essentials (arrays, tasks/functions, assertions) in testbench code.	Apply
CO3	Create reusable OOP-based components (classes, dynamic objects) following best practices.	Create
CO4	Analyze and coordinate concurrent processes (fork-join, events, mailboxes, semaphores) for synchronization.	Analyze
CO5	Evaluate functional coverage results to guide further test development and achieve closure.	Evaluate

Mapping with Programme Outcomes

COs	POs					
	1	2	3	4	5	6
CO1	3	3	3	2	2	3
CO2	3	3	3	2	2	3
CO3	3	3	3	2	2	3
CO4	3	3	3	2	2	3
CO5	3	3	3	2	2	3
3 - Strong; 2 - Medium; 1 - Some						

Bloom's Category	Continuous Assessment Tests (Marks)				Model Examination (Marks)	End Sem Examination (Marks)	
	Test 1		Test 2				
	Theory	Lab	Theory	Lab	Lab	Theory	Lab
Remember	-	-	-	-	-	20	-
Understand	30	10	30	10	10	60	10
Apply	30	90	30	90	90	20	90
Analyse	-	-	-	-	-	-	-
Evaluate	-	-	-	-	-	-	-
Create	-	-	-	-	-	-	-

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Total	60	100	60	100	100	100	100

Syllabus

K.S.Rangasamy College of Technology – Autonomous R2025							
M.E-VLSI Design							
70 PVL E51- System Verilog							
Semester	**Hours/Week**			**Total Hours**	**Credit**	**Maximum Marks**	
	L	T	P		C	CA	ES	Total
III	3	0	2	75	4	50	50	100

Advanced Verification Methodology* Introduction to Functional Verification, Verification Process and Planning, Directed vs. Constrained-Random Testing, Layered Test bench Architecture, Overview of System Verilog Verification Methodologies (OVM, UVM), Functional Coverage Basics and Goals, Components of a Modern Test bench: Driver, Monitor, Scoreboard, Agent	[9]
System Verilog Language Essentials Built-in and User-defined Data Types, Packed vs. Unpacked Arrays, Queues, Dynamic Arrays, Associative Arrays, Typedefs, Enums, Structures, and Unions, Constants, Strings, and System Verilog Assertions (intro), Procedural Code: Initial, Always, Fork- Join, Tasks and Functions (void, automatic, local variables)	[9]
Object-Oriented Programming in System Verilog Classes and Object Creation, Class Inheritance and Polymorphism, Constructors and Destructors, Dynamic Objects and Shallow/Deep Copy, Encapsulation: Public, Private, Local, Scope Resolution and Static Variables, Creating and Managing Multiple Objects, OOP Best Practices in Test bench Design	[9]
Concurrency, Inter-Process Communication, and Functional Coverage Fork-Join and Threading Concepts, Events, Mailboxes, Semaphores, Inter-process Synchronization in Test benches, Functional Coverage Concepts and Goals, Covergroups, Coverpoints, Cross Coverage, Parameterized Covergroups, Coverage Data Analysis and Reporting, Building Coverage-Driven Test benches	[9]
Case Study – Complete System Verilog Verification Environment** Case Study: Design and Verification of ATM Module, Interface and Modport Design, Virtual Interfaces and Encapsulation, Top-Level Design Integration, Test bench Components: Generator, Driver, Monitor, Scoreboard, Test Scenarios and Coverage Collection, Reusability and Maintainability Practices Practical: 1. Design a Test bench for 2x1 Mux Using Gates 2. Implementation of a Mailbox by Allocating Memory 3. Implementation and Testing of Semaphore for a Simple DUT 4. Implementation of Scoreboard for a Simple DUT	[9]
Total Hours: (Lecture – 45; Practical -30)	75

Text book(s):	
1	Chris Spear, “System Verilog for Verification: a Guide to Learning The Test bench Language Features”, Springer, 2016.
2	UVM — ”Buyer’s Guide and Verification Methodology”, Janick Bergeron, Springer, 2015
Reference(s):	
1	Stuart Sutherland, Simon Davidman and Peter Flake, “System Verilog for Design: a Guide to Using

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	System Verilog for Hardware Design and Modeling", 2nd Edition, Springer,
2	Ashok B. Mehta and Alexandru Duta, Wiley "Functional Verification Coverage Measurement and Analysis", -IEEE Press, 2015
3	Shawn Honess & Sagar R. Gupta , "Practical UVM: A Guide to Building a Universal Verification Methodology Testbench", VHDL Insights, 2016

* SDG 4 – Quality Education
** SDG 9 – Industry, Innovation, and Infrastructure

Passed in BoS Meeting held on 13/06/2025
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Department of ECE
K.S.Rangasamy College of Technology

Course Contents and Lecture Schedule

S. No.	Topics	No. of hours
1	**Advanced Verification Methodology**	
1.1	Introduction to Functional Verification,	1
1.2	Verification Process and Planning,	1
1.3	Directed vs. Constrained-Random Testing,	1
1.4	Layered Test bench Architecture,	1
1.5	Overview of System Verilog Verification Methodologies (OVM)	1
1.6	Overview of System Verilog Verification Methodologies (UVM),	1
1.7	Functional Coverage Basics and Goals,	1
1.8	Components of a Modern Test bench: Driver, Monitor	1
1.9	Components of a Modern Test bench: Scoreboard, Agent	1
2	**System Verilog Language Essentials**	
2.1	Built-in and User-defined Data Types	1
2.2	Packed vs. Unpacked Arrays	1
2.3	Queues	1
2.4	Dynamic Arrays	1
2.5	Associative Arrays	1
2.6	Typedefs, Enums, Structures, and Unions, Constants, Strings	1
2.7	System Verilog Assertions (intro)	1
2.8	Procedural Code: Initial, Always, Fork-Join	1
2.9	Tasks and Functions (void, automatic, local variables)	1
3	**Object-Oriented Programming in System Verilog**	
3.1	Classes and Object Creation	1
3.2	Class Inheritance and Polymorphism	1
3.3	Constructors and Destructors	1
3.4	Dynamic Objects	1
3.5	Shallow/Deep Copy	1
3.6	Encapsulation: Public, Private, Local	1
3.7	Scope Resolution and Static Variables	1
3.8	Creating and Managing Multiple Objects	1
3.9	OOP Best Practices in Testbench Design	1
4	**Concurrency, Inter-Process Communication, and Functional Coverage**	
4.1	Fork-Join and Threading Concepts	1
4.2	Events, Mailboxes, Semaphores	1
4.3	Inter-process Synchronization in Testbenches	1
4.4	Functional Coverage Concepts and Goals,	1
4.5	Cover groups, Cover points	1
4.6	Cross Coverage	1

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4.7	Parameterized Cover groups	1
4.8	Coverage Data Analysis and Reporting	1
4.9	Building Coverage-Driven Testbenches	1
5	**Case Study – Complete System Verilog Verification Environment**	
5.1	Design and Verification of ATM Module,	1
5.2	Interface and Modport Design,	1
5.3	Virtual Interfaces and Encapsulation,	1
5.4	Top-Level Design Integration,	1
5.5	Testbench Components: Generator, Driver	1
5.6	Testbench Components: Monitor, Scoreboard,	1
5.7	Test Scenarios and Coverage Collection,	1
5.8	Reusability Practices	1
5.9	Maintainability Practices	1
Practical:		
1.	Design a Testbench for 2x1 Mux Using Gates	7
2.	Implementation of a Mailbox by Allocating Memory	8
3.	Implementation and Testing of Semaphore for a Simple DUT	7
4.	Implementation of Scoreboard for a Simple DUT	8

Course Designer(s)

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70 PVL E52	HDL for IC Design	Category	L	T	P	Credit
		PE	3	0	2	4

Objectives

- To understand the basics of Verilog HDL
- To design digital systems using the different modeling
- To understand the HDL synthesis
- To learn verification process
- To test the design using testbench

Pre-requisites

- Design System Design, Verilog HDL

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Apply digital design concepts and write Verilog programs	Apply
CO2	Write Verilog programs using dataflow and behavioral modeling	Apply
CO3	Synthesis the digital design for implementation in FPGA	Apply
CO4	Understand the principles of verification process and System Verilog	Apply
CO5	Interface test bench and design under test	Apply

Mapping with Programme Outcomes

COs	POs					
	1	2	3	4	5	6
CO1	3	3	3	3	3	3
CO2	3	3	3	3	3	3
CO3	3	3	3	3	3	3
CO4	3	3	3	3	3	3
CO5	3	3	3	3	3	3
3 - Strong; 2 - Medium; 1 - Some						

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)				Model Examination (Marks)	End Sem Examination (Marks)	
	Test 1		Test 2				
	Theory	Lab	Theory	Lab	Lab	Theory	Lab
Remember	-	-	-	-	-	20	-
Understand	30	10	30	10	10	60	10
Apply	30	90	30	90	90	20	90
Analyse	-	-	-	-	-	-	-
Evaluate	-	-	-	-	-	-	-
Create	-	-	-	-	-	-	-
Total	60	100	60	100	100	100	100

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Syllabus

K.S.Rangasamy College of Technology – Autonomous R2025

M.E-VLSI Design

70 PVL E52- HDL for IC Design

Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
III	3	0	2	75	4	50	50	100

Introduction to Verilog Overview of Digital Design using Verilog HDL-Hierarchical Modeling Concepts-Verilog Operators and Modules-Verilog Ports, Data types and Assignments-Gate level modeling-Switch level modeling-Modeling of CMOS Gates and Boolean Functions.	[9]
Dataflow and Behavioral modeling Basics of dataflow modeling-Review of flip-flops-Verilog modeling of Flip-Flops-Basics of Behavioral Modeling-Verilog Modeling of Counters, Sequence Detector, FSMs and Shift Registers.	[9]
Verilog HDL Synthesis* Synthesis Design Flow-Verification of the Gate Level Net List-Modeling for Logic Synthesis-Example of Sequential Circuit Synthesis - FIR Filter Implementation-IIR filter Implementation.	[9]
Introduction to System Verilog** Verification Process- Basic Testbench Functionality - Directed Testing - Constrained-Random Stimulus, Functional Coverage, Testbench Components- Layered Testbench- Building a Layered Testbench- Simulation Environment Phases - Data types and procedural statements: Built-In Data Types- Fixed-Size Arrays- Dynamic Arrays- Queues- Associative Arrays- Array Methods- Choosing a Storage Type- Creating New Types with typedef- Creating User-Defined Structures- Type conversion- Enumerated Types- Task and Function Overview- Routine Arguments- Returning from a Routine.	[9]
Connecting the Test bench and Design Separating the Test bench and Design-The Interface Construct-Stimulus Timing-Interface Driving and Sampling-Connecting It All Together-Top-Level Scope-Program - Module Interactions-System Verilog Assertions-The Four-Port ATM Router.	[9]
Practical: 1. Simulate the Combinational Circuits using Different Modeling 2. Design and Implement FSM 3. Design and Implement FIR and IIR filter 4. Verify the Digital Systems using System Verilog 5. Design and implement a System verilog test bench to verify a Four-Port ATM Router	[30]
Total Hours: (Lecture - 45; Practical - 30)	75

Text book(s):

1	Samir Palnitkar, "Verilog HDL: A Guide to Digital Design and Synthesis", 2nd Edition, Pearson Education New Delhi, 2019
2	Chris Spear, "System Verilog for Verification: A Guide to Learning the Test bench Language Features", 2nd Edition, Springer, 2018.

Reference(s):

1	https://ocw.mit.edu - Massachusetts Institute of Technology Open Courseware.
2	Michael D Ciletti , "Advanced Digital Design with the Verilog HDL", 2nd Edition, PHI, 2019
3	Stephen Brown and Zvonko Vranesic, " Fundamentals of Digital Logic with Verilog", 2nd Edition, TMH, 2018

*SDG 9 – Industry, Innovation, and Infrastructure
**SDG 7 – Affordable and Clean Energy

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Course Contents and Lecture Schedule		
S. No.	**Topics**	**No. of hours**
1.0	**Verification Methodology**	
1.1	Overview of digital design using Verilog HDL	1
1.2	Hierarchical Modeling concepts	1
1.3	Verilog Operators and Modules	1
1.4	Verilog Ports, Data types and Assignments	1
1.5	Gate level modelling	1
1.6	Switch level modelling	1
1.7	Modelling of CMOS gates	1
1.8	Boolean functions	2
2.0	**Dataflow and behavioral modelling**	
2.1	Basics of dataflow modelling	1
2.2	Review of flip-flops	1
2.3	Verilog modeling of flip-flops	2
2.4	Basics of behavioral modelling	1
2.5	Verilog modeling of counters	1
2.6	Sequence Detector	1
2.7	Finite State Machine (FSM)	1
2.8	Shift Registers	1
3.0	**Verilog HDL Synthesis**	
3.1	Synthesis Design Flow	1
3.2	Verification of the gate level net list	4
3.3	Modeling for logic synthesis	1
3.4	Example of sequential circuit synthesis	1
3.5	FIR filter implementation-IIR filter implementation	2
4.0	**Introduction to System Verilog**	
4.1	Verification Process- Basic Testbench Functionality	1
4.2	Directed Testing - Constrained-Random Stimulus	1
4.3	Functional Coverage, Testbench Components	1
4.4	Layered Testbench- Building a Layered Testbench	1
4.5	Simulation Environment Phases	1
4.6	Data types and procedural statements: Built-In Data Types	1
4.7	Fixed-Size Arrays- Dynamic Arrays- Queues- Associative Arrays	1
4.8	Array Methods- Choosing a Storage Type- Creating New Types with typedef- Creating User-Defined Structures- Type conversion	1
4.9	Enumerated Types- Task and Function Overview- Routine Arguments- Returning from a Routine	1
5.0	**Connecting the Test bench and Design**	
5.1	Separating the Test bench and Design	1
5.2	The Interface Construct	1
5.3	Stimulus Timing	1
5.4	Interface Driving	1
5.5	Sampling-Connecting It All Together	1

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5.6	Top-Level Scope-Program	1
5.7	Module Interactions	1

5.8	System Verilog Assertions	1
5.9	The Four-Port ATM Router	1
Practical:		
1.	Simulate the Combinational Circuits using Different Modeling	7
2.	Design and Implement FSM	8
3.	Design and Implement FIR and IIR filter	7
4.	Verify the Digital Systems using System Verilog	8

Course Designer(s)

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70 PVL E53	Deep Learning	Category	L	T	P	Credit
		PE	3	0	2	4

Objectives

- To present the mathematical, statistical and computational challenges of building neural Networks,
- To study the concepts of back propagation & optimization algorithms,
- To introduce dimensionality reduction techniques,
- To study different deep neural networks and
- To study the optimization of deep networks

Pre-requisites

- Machine Learning Techniques

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Design and develop deep neural network	Apply
CO2	Design, implement, and optimize deep autoencoder-based models for unsupervised feature extraction	Apply
CO3	Design, implement, and optimize Deep Stacking Networks (DSNs) and their variants	Apply
CO4	Explain the architecture of different DNN	Understand
CO5	Study the generator and discriminator components of GAN	Understand

Mapping with Programme Outcomes

COs	POs					
	1	2	3	4	5	6
CO1	3	-	2	-	2	3
CO2	3	-	3	2	3	3
CO3	3	-	3	2	3	3
CO4	3	-	3	2	3	3
CO5	3	-	3	2	3	3
3 - Strong; 2 - Medium; 1 - Some						

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)				Model Examination (Marks)	End Sem Examination (Marks)	
	Test 1		Test 2				
	Theory	Lab	Theory	Lab	Lab	Theory	Lab
Remember	10	-	10	-	-	30	-
Understand	20	10	20	10	10	30	10
Apply	20	80	20	80	70	30	80
Analyse	10	10	10	10	20	10	10
Evaluate	-	-	-	-	-	-	-
Create	-	-	-	-	-	-	-
Total	60	100	60	100	100	100	100

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Syllabus

K.S.Rangasamy College of Technology – Autonomous R2025								
M.E-VLSI Design								
70 PVL E53- Deep Learning								
Semester	**Hours/Week**			**Total Hours**	**Credit**	**Maximum Marks**		
	L	T	P		C	CA	ES	Total
III	3	0	2	75	4	50	50	100

Deep Learning Networks A Three-Way Categorization, Deep Networks for Unsupervised or Generative Learning, Deep Networks for Supervised Learning, Hybrid Deep Networks, Regularization, Optimization in Deep Learning, Data set Augmentation, Dropout.	[9]
Deep Autoencoders and Unsupervised Learning Use Of Deep Autoencoders To Extract Speech Features, Stacked Denoising Autoencoders, Transforming Autoencoders, Restricted Boltzmann Machines, Unsupervised Layer-Wise Pre-Training, Interfacing DNNs with HMMs, Attention & Transformers, Selected Applications in Speech and Audio Processing	[9]
Deep Stacking Networks and Variants and Supervised Learning* A Basic Architecture Of The Deep Stacking Network, A Method For Learning The DSN Weights, The Tensor Deep Stacking Network, The Kernelized Deep Stacking network, Selected Applications in Object Recognition and Computer Vision	[9]
Deep Convolution Neural Networks Architectures — AlexNet, VGGNet, DenseNet, ResNet - Training a: Weights Initialization, Batch Normalization, RCNN and YOLO architectures, Fully Convolutional Segmentations, Mask-RCNNs, LSTM	[9]
Generative Models** Autoregressive Models, Variational auto Encoders, Reversible Flow, Generative Adversarial Networks- Building Blocks, Strength and Weakness, Implementing Generator and Discriminator.	[9]
Practical: 1. Study the effect of batch normalization and dropout in neural network classifier 2. Google speech recognition using microphone input 3. Movie recommendations on Netflix/product recommendations on Amazon 4. Image segmentation using VGGNet 5. Generate handwritten digits similar to those in the MNIST dataset	[30]
Total Hours: (Lecture - 45; Practical - 30)	75

Text book(s):	
1	Deng & Yu, Deep Learning: "Methods and Applications", Now Publishers, 2018
2	Ian Goodfellow, Yoshua Bengio, Aaron Courville, "Deep Learning", MIT Press, 2016
Reference(s):	
1.	Michael Nielsen, "Neural Networks and Deep Learning", Determination Press, 2015
2.	Cosma Rohilla Shalizi, "Advanced Data Analysis from an Elementary Point of View", 2015
3.	Francois Chollet, "Deep learning with Python" – Manning Publications

*SDG 9 – Industry, Innovation, and Infrastructure

**SDG 3 – Good Health and Well-being

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Course Contents and Lecture Schedule

S.No	Topics	No.of Hours
1	**Deep Learning Networks**	
1.1	A three-way categorization	1
1.2	Deep networks for unsupervised or generative learning	1
1.3	Deep networks for supervised learning	1
1.4	Hybrid deep networks	1
1.5	Regularization	2
1.6	Optimization in deep learning	1
1.7	Data set Augmentation, Dropout	2
1.8	Practical: Study the effect of batch normalization and dropout in neural network classifier	3
2	**Deep Autoencoders — Unsupervised Learning**	
2.1	Use of deep autoencoders to extract speech features	1
2.2	Stacked denoising autoencoders	1
2.3	Transforming autoencoders	1
2.4	Pre-Trained Deep Neural Networks — A Hybrid, Restricted Boltzmann machines	2
2.5	Unsupervised layer-wise pre-training	1
2.6	Interfacing DNNs with HMMs	1
2.7	Attention & transformers	1
2.8	Selected Applications in Speech and Audio Processing	1
2.9	Practical: Google speech recognition using microphone input	3
3	**Deep Stacking Networ2ks and Variants —Supervised Learning**	
3.1	A basic architecture of the deep stacking network	2
3.2	A method for learning the DSN weights	2
3.3	The tensor deep stacking network	1
3.4	The Kernelized deep stacking network	2
3.5	Selected Applications in Object Recognition and Computer Vision	2
3.6	Practical: Movie recommendations on Netflix/product recommendations on Amazon	3
4	**Deep Convolution Neural Networks**	
4.1	Architectures – AlexNet,	1
4.2	VGGNet	1
4.3	DenseNet	1
4.4	ResNet - Training a: weights initialization, batch normalization	1
4.5	RCNN	1
4.6	YOLO architectures	1
4.7	Fully convolutional segmentations	1
4.8	Mask-RCNNs, LSTM	2
4.9	Practical: Image segmentation using VGGNet	3
5	**Generative Models**	

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5.1	Autoregressive models	1
5.2	Variational auto encoders	2
5.3	Reversible flow	1
5.4	Generative Adversarial Networks	1
5.5	Building blocks, Strength and weakness	2
5.6	Implementing generator and discriminator.	2
5.7	Practical: Generate handwritten digits similar to those in the MNIST dataset	3
Practicals:		
1.	Study the effect of batch normalization and dropout in neural network classifier	7
2.	Google speech recognition using microphone input	8
3.	Movie recommendations on Netflix/product recommendations on Amazon	4
4.	Image segmentation using VGGNet	4
5.	Generate handwritten digits similar to those in the MNIST dataset	7

Course Designer(s)

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70 PVL E54	Adaptive Signal Processing	Category	L	T	P	Credit
		PE	3	0	2	4

Objectives

- To understand the concepts of stationary and non-stationary random signals and characterization of discrete-time random processes.
- To explain Non parametric and parametric methods for power spectrum estimation.
- To design optimum filters such as Wiener and Kalman filters.
- To design adaptive filtering techniques using LMS and RLS algorithm and understand the applications of adaptive filters.
- To learn the concepts of Continuous Wavelet, Transform and its applications

Pre-requisites

- Digital Signal Processing

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Explain the mathematical description and signal modelling of discrete	Apply
CO2	Apply various techniques for estimating the power spectrum of a	Apply
CO3	Design different optimum filters	Analyse
CO4	Design, implementation and analysis of FIR adaptive filters and	Analyse
CO5	Discuss the concepts of CWT and its applications.	Understand

Mapping with Programme Outcomes

COs	POs					
	1	2	3	4	5	6
CO1	3	3	-	3	3	-
CO2	3	3	-	-	3	3
CO3	3	3	3	3	3	3
CO4	3	3	3	3	3	3
CO5	3	3	-	-	3	-
3 - Strong; 2 - Medium; 1 - Some						

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)				Model Examination (Marks)	End Sem Examination (Marks)	
	Test 1		Test 2				
	Theory	Lab	Theory	Lab	Lab	Theory	Lab
Remember	20	-	10	-	-	30	-
Understand	20	10	20	10	10	30	10
Apply	20	80	20	80	70	30	80
Analyse	10	10	10	10	20	10	10
Evaluate	-	-	-	-	-	-	-
Create	-	-	-	-	-	-	-
Total	60	100	60	100	100	100	100

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Syllabus

K.S.Rangasamy College of Technology – Autonomous R2025

M.E-VLSI Design

70 PVL E54 - Adaptive Signal Processing

Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
III	3	0	2	75	4	50	50	100

Discrete time Random Signals Discrete Random Processes-Definitions-Ensemble Averages-Stationary Processes-Auto Covariance and Autocorrelation Matrices-Properties- Ergodicity- White noise-Weiner Khitchine Relation- Power Spectral Density –Filtering Random Processes-Spectral Factorization Theorem- Special Types of Random Processes – ARMA, AR, MA Processes-Pade approximation – Prony's method.	[9]
Spectrum Estimation Non-Parametric Methods: Periodogram - Performance of the Periodogram, Modified Periodogram, Barlett'smethod, Welch's Method and Blackman-Tukey Approach-Performance comparisons -Parametric methods - AR, MA, ARMA Spectrum Estimation using YuleWalker Method- the Levinson-Durbin Recursion- Development of the Recursion-The Levinson Recursion Algorithm for Solving Toeplitz System of Equations	[9]
Optimum Filters Linear Minimum Mean-Square Error (LMMSE) Filtering: Wiener Hopf Equation, FIR Wiener Filter-Filtering, Linear Prediction- IIR Wiener filter-Causal and Non causal IIR Wiener filter-Discrete Kalman Filter.	[9]
Adaptive Filters* FIR Adaptive filters - Newton's steepest descent method - Widrow-Hoff LMS Adaptive algorithm -Normalized LMS Algorithm- Applications - Noise cancellation - Channel equalization — Echo cancellation- Adaptive Recursive Filters - RLS adaptive algorithm	[9]
Continuous Wavelet Transforms** Wavelet basis– STFT- Continuous time Wavelet Transform (CWT)– Principles of Multi-Resolution Analysis (MRA) - Construction of Wavelets-Construction of Orthonormal Wavelets-Applications of Wavelet Transform - Noise Reduction, Image Compression.	[9]
Practical: 1. Power Spectral Density using Square Magnitude and Autocorrelation Method 2. Estimate the PSD of a Noisy Signal using Periodogram and Modified Periodogram. 3. Application of Optimum Filters 4. Adaptive Filter for Noise Cancellation in Sinusoidal Signal and System Identification using Adaptive filter 5. Time-Frequency Analysis with the Continuous Wavelet Transform and Signal Reconstruction from continuous Wavelet Transform Coefficients	[30]
Total Hours: (Lecture - 45; Practical - 30)	75

Text book(s):

1	Monson H. Hayes, "Statistical Digital Signal Processing and Modeling", John Wiley and Sons Inc., New York, 2008.
2	Jaideva C Goswami and Andrew K Chan, "Fundamentals of Wavelets–Theory, Algorithms and Applications", John Wiley &Sons, Inc., Singapore, 2011.

Reference(s):

1.	Alan V Oppenheim, Ronald W Schafer, "Discrete Time Signal Processing", Pearson Education India, 3rd Edition, 2014.
2.	John G. Proakis, Dimitris G. Manolakis, "Digital Signal Processing: Principles, Algorithms and Applications", 4th Edition, Pearson Education,2014.
3.	Simon Haykin, "Adaptive Filter Theory", 5th Edition, Pearson, 2013.
4.	Steven M.Kay, "Modern Spectrum Estimation: Theory and Application", Prentice Hall PTR, 2015.

*SDG 9 – Industry, Innovation, and Infrastructure

**SDG 3 – Good Health and Well-being

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Course Contents and Lecture Schedule		
S. No.	**Topics**	**No. of Hours**
1.0	**Discrete time Random Signals**	
1.1	Discrete Random Processes Definitions	1
1.2	Ensemble Averages,Stationary processes	1
1.3	Auto Covariance and Autocorrelation Matrices-Properties Ergodicity	1
1.4	White Noise Weiner Khitchine relation Power Spectral Density	1
1.5	Filtering Random Processes: Spectral Factorization Theorem	1
1.6	Special types of Random Processes	1
1.7	ARMA, AR, MA Processes	1
1.8	Pade Approximation	1
1.9	Prony's Method.	1
2.0	**Spectrum Estimation**	
2.1	Non-Parametric Methods: Periodogram Performance of the Periodogram	1
2.2	Modified Periodogram	1
2.3	Barlett's Method	1
2.4	Welch's Method and Blackman-Tukey Approach Performance Comparisons	1
2.5	Parametric Methods: AR, MA, ARMA Spectrum	1
2.6	Estimation using Yule Walker Method	1
2.7	The Levinson-Durbin Recursion	1
2.8	Development of the Recursion	1
2.9	The Levinson Recursion Algorithm for Solving Toeplitz System of Equations.	1
3.0	**Optimum Filters**	
3.1	(LMMSE) Filtering: Wiener Hopf Equation	2
3.2	FIR Wiener Filter	1
3.3	Filtering & Linear Prediction	1
3.4	IIR Wiener Filter	1
3.5	Causal IIR Wiener Filter	1
3.6	Non causal IIR Wiener Filter	1
3.7	Discrete Kalman Filter.	2
4.0	**Adaptive Filters**	
4.1	FIR Adaptive Filters	1
4.2	Newton's Steepest Descent Method	1
4.3	Widrow-Hoff LMS Adaptive Algorithm	1
4.4	Normalized LMS Algorithm	1
4.5	Noise Cancellation	1
4.6	Channel Equalization	1
4.7	Echo Cancellation	1
4.8	Adaptive Recursive Filters: RLS Adaptive Algorithm	2
5.0	**Continuous Wavelet transform**	

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5.1	Wavelet Basis STFT	1

5.2	Continuous Time Wavelet Transform (CWT)	2
5.3	Principles of Multi-Resolution Analysis (MRA)	1
5.4	Construction of Wavelets	1
5.5	Construction of Orthonormal Wavelets	1
5.6	Applications of Wavelet transform: Noise Reduction, Image Compression.	2
Practical:		
1.	Power Spectral Density using Square Magnitude and Autocorrelation Method	6
2.	Estimate the PSD of a Noisy Signal using Periodogram and Modified Periodogram.	6
3.	Application of Optimum Filters	6
4.	Adaptive Filter for Noise Cancellation in Sinusoidal Signal and System Identification using Adaptive filter	6
5.	Time-Frequency Analysis with the Continuous Wavelet Transform and Signal Reconstruction from continuous Wavelet Transform Coefficients	6

Course Designer(s)

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70 PVL E55	MEMS System Design	Category	L	T	P	Credit
		PE	3	0	2	4

Objectives

- To introduce and provide a broad view of MEMS and micro systems.
- To familiarize with the fundamentals of MEMS products, materials for microsystems
- To learn the microsystem fabrication process
- To learn the various MEMS-specific design issues and constraints will be discussed in detail
- To know the applications of micro sensors and micro actuators

Pre-requisites

- Electronic Circuits

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Know the basic principles of MEMS sensors and actuators.	Understand
CO2	Outline the various materials used for MEMS products.	Analyse
CO3	Familiarize with the fabrication process of MEMS devices.	Analyse
CO4	Analyze the design process in mems systems.	Analyse
CO5	Know the diverse applications of MEMS sensors	Understand

Mapping with Programme Outcomes

COs	POs					
	1	2	3	4	5	6
CO1	3	3	3	-	-	-
CO2	3	3	3	-	-	3
CO3	3	-	3	-	3	3
CO4	3	3	3	3	-	-
CO5	3	3	3	-	3	3
3 - Strong; 2 - Medium; 1 - Some						

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)				Model Examination (Marks)	End Sem Examination (Marks)	
	Test 1		Test 2				
	Theory	Lab	Theory	Lab	Lab	Theory	Lab
Remember	10	-	10	-	-	30	-
Understand	10	10	20	10	10	25	10
Apply	20	70	20	70	70	30	70
Analyse	20	20	10	20	20	15	20
Evaluate	-	-	-	-	-	-	-
Create	-	-	-	-	-	-	-
Total	60	100	60	100	100	100	100

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Syllabus

K.S.Rangasamy College of Technology – Autonomous R2025

M.E-VLSI Design

70 PVL E55– MEMS System Design

Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
III	3	0	2	75	4	50	50	100

Introduction Overview -MEMS and Micro System Products-Microsystems and Microelectronics - Working Principle of Microsystems-Micro Actuation Techniques.	[9]
Materials for Microsystems Substrate and Wafer- Single Crystal Silicon Wafer Formation- Ideal Substrates- Mechanical Properties- Silicon Compounds-Sio2, SiC, Si3N4 and Polycrystalline Silicon-Silicon Piezo Resistors-Gallium Arsenide -Quartz-Piezoelectric Crystals - Polymers.	[9]
Micro System Fabrication Process Photolithography – Photo Resist- Ion Implantation – Diffusion – Oxidation – CVD – Physical Vapor Deposition- Deposition by Epitaxy – Etching Process.	[9]
Micro System Design Design Considerations- Process Design- Mask Layout Design- Design Constraints- Selection of Materials-Manufacturing Process - Signal Transduction-Packaging – Application of Micro System in Automotive Industry-Biomedical-Aerospace-Telecommunication.	[9]
Micro Sensors Introduction- Microsensors- Biomedical Sensors- Pressure Sensors- Thermal Sensors–Chemical Sensors– Optical Sensors–Microactuation– MEMS with Actuators.	[9]
Practical: 1. Design and Analysis of Capacitive Accelerometer 2. Estimation of Resistance change in SOI Piezo-Resistive Pressure Sensor 3. Study of IntelliSuite Software for the Design and Fabrication Process of MEMS devices 4. Design and Analysis of Piezoresistive Accelerometer using Coventor Ware Software. 5. Simulation of Microsensors	[30]
Total Hours: (Lecture - 45; Practical - 30)	75

Text book(s):

1	Tai-Ran Hus, "MEMS & Microsystems Design, Manufacture and Nanoscale engineering", John Wiley & Sons, 2013.
2	Julian W.Gardner, Vijay K.Varadan, Osama O.Awadel Karim, "Microsensors MEMS and Smart Devices", John Wiley & sons, 2011.

Reference(s):

1.	Chang Liu, "Foundations of MEMS", Pearson Education Inc., 2012.
2.	Stephen D Senturia, "Microsystem Design", Springer Publication, 2000.
3.	James J.Allen, "Micro Electro Mechanical System Design", CRC Press Publisher, 2005.
4.	Thomas M.Adams and Richard A.Layton, "Introduction MEMS, Fabrication and Application", Springer,2010.

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Course Contents and Lecture Schedule		
S. No.	**Topics**	
1.0	**Introduction**	
1.1	Overview	1
1.2	MEMS	1
1.3	Microsystems	1
1.4	Micro System Products	1
1.5	Microelectronics	1
1.6	Compare Microelectronics and Microsystems	1
1.7	Working Principle of Microsystems	1
1.8	Micro Actuation Techniques	1
1.9	Applications of MEMS	1
2.0	**Materials for Microsystems**	
2.1	Substrate and Wafer	1
2.2	Single Crystal Silicon Wafer Formation	1
2.3	Ideal Substrates	1
2.4	Mechanical Properties	1
2.5	Silicon Compounds	1
2.6	Sio2, SiC, Si3N4 and Polycrystalline Silicon	1
2.7	Silicon Piezo Resistors	1
2.8	Gallium Arsenide, Quartz	1
2.9	Piezoelectric Crystals, Polymers	1
3.0	**Micro System Fabrication Process**	
3.1	Photolithography	1
3.2	Photo Resist	1
3.3	Ion Implantation	1
3.4	Diffusion	1
3.5	Oxidation	1
3.6	CVD	1
3.7	Physical Vapor Deposition	1
3.8	Deposition by Epitaxy	1
3.9	Etching Process	1
4.0	**Micro System Design**	
4.1	Design Considerations	1
4.2	Process Design	1
4.3	Mask Layout Design	1
4.4	Design Constraints, Selection of Materials	1
4.5	Manufacturing Process	1
4.6	Signal Transduction, packaging	1
4.7	Application of Micro System in Automotive Industry	1
4.8	Biomedical	1
4.9	Aerospace, Telecommunication.	1

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5.0	**Micro Sensors**	
5.1	Introduction	1
5.2	Microsensors	1
5.3	Biomedical Sensors	1
5.4	Pressure Sensors	1
5.5	Thermal Sensors	1
5.6	Chemical Sensors	1
5.7	Optical Sensors	1
5.8	Micro actuation	1
5.9	MEMS with Actuators	1
Practical:		
1.	Design and Analysis of Capacitive Accelerometer	6
2.	Estimation of Resistance Change in SOI Piezo-Resistive Pressure Sensor	6
3.	Study of IntelliSuite Software for the Design and Fabrication Process of MEMS devices	6
4.	Design and Analysis of Piezoresistive Accelerometer using Coventor Ware Software.	6
5.	Simulation of Microsensors	6

Course Designer(s)

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70 PVL 3P1	Project Work - Phase I	Category	L	T	P	Credit
		CG	0	0	12	6

Objectives

- To impart practical knowledge to the students and also to make them to carry out the technical procedures in their project work.
- To provide an exposure to the students to refer, read and review the research articles, journals and conference proceedings relevant to their project work and placing this as their beginning stage for their final presentation
- Independently carry out research / investigation and development work to solve practical problems in the field of VLSI
- Write and present a substantial technical report / document in the field of VLSI
- Demonstrate the Research findings the VLSI area

Pre-requisites

- Nil

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Survey the relevant literature such as books, national/international referred journals and contact resource persons for the selected topic of research.	Apply
CO2	Use different experimental techniques/different software/ Computational / analytical tools.	Apply
CO3	Design and develop an experimental set up/ equipment/test rig.	Apply
CO4	Conduct tests on existing setups/equipment's and draws logical conclusions from the results after analyzing them.	Apply
CO5	Work in a research environment or in an industrial environment	Apply

Mapping with Programme Outcomes

COs	POs					
	1	2	3	4	5	6
CO1	3	3	3	3	3	3
CO2	3	3	3	3	3	3
CO3	3	3	3	3	3	3
CO4	3	3	3	3	3	3
CO5	3	3	3	3	3	3
3 - Strong; 2 - Medium; 1 - Some						

Assessment Pattern

(Internal Assessment: 100 Marks)

Review I (R1)			Review II (R2)		Review III (R3)			Total (R1+R2+R3)	Internal
Literature Survey	Topic Identification & Justification	Work Plan	Approach	Conclusion	Demo-Existing System	Presentation	Report	Total	
10	10	10	20	20	10	10	10	100	100

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M.E-VLSI Design								
70 PVL 3P1 - Project Work - Phase I								
Semester	Hours/Week			Total Hrs	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
III	0	0	12	180	6	100	-	100

Methodology:

- Project should be selected based on an IEEE paper which would be base paper
- The paper has to be implemented fully
- Modification has to be proposed on the base paper
- Report has to be prepared by the students as per the format
- Every week a report on the progress of the project has to be submitted (Friday/Saturday) by the student with the supervisor's signature
- Three reviews will be conducted by a committee of minimum three members one of which should be the guide
- Each review has to be evaluated for 100 marks
- Attendance is compulsory for all reviews. If a student fails to attend the review for some valid reason with proper intimation, one or more chance may be given, else review mark will be zero
- Internal evaluation has to be done for 100 marks

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K.S. RANGASAMY COLLEGE OF TECHNOLOGY, TIRUCHENGODE - 637215
(An Autonomous Institution affiliated to Anna University)

M.E. / M.Tech. Degree Programme

SCHEME OF EXAMINATIONS

(For the candidates admitted in 2025-2026)

FOURTH SEMESTER

S.No.	Course Code	Name of the Course	Duration of Internal Exam	Weightage of Marks			Minimum Marks for Pass in End Semester Exam	
				Continuous Assessment *	End Semester Exam **	Max. Marks	End Semester Exam	Total
PRACTICAL								
1.	70 PVL 4P1	Project Work - Phase II	3	60	40	100	45	100

* CA evaluation pattern will differ from course to course and for different tests. This will have to be declared in advance to students. The department will put a process in place to ensure that the actual test paper follow the declared pattern.

** End Semester Examination will be conducted for maximum marks of 100 and subsequently be reduced to 40 marks for project End semester Examinations.

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70 PVL 4P1	Project Work - Phase II	Category	L	T	P	Credit
		CG	0	0	24	12

Objectives

- To impart practical knowledge to the students and also to make them to carry out the technical procedures in their project work.
- To provide an exposure to the students to refer, read and review the research articles, journals and conference proceedings relevant to their project work and placing this as their beginning stage for their final presentation
- Independently carry out research / investigation and development work to solve practical problems in the field of VLSI
- Write and present a substantial technical report / document in the field of VLSI
- Demonstrate the Research findings the VLSI area

Pre-requisites

- Nil

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Develop attitude of lifelong learning and interpersonal skills to deal with people working in diversified fields.	Apply
CO2	Synthesize knowledge and skills previously gained and apply to an in-depth study and execution of new technical problems in the area of VLSI.	Apply
CO3	Define specification, adopt new VLSI methodologies and analyze to produce a suitable research design and justify the design.	Apply
CO4	Demonstrate the research findings through hardware and software tools.	Apply
CO5	Present the findings of their technical solution in a written report and Publish the work in reputed journals and International Conferences.	Apply

Mapping with Programme Outcomes

COs	POs					
	1	2	3	4	5	6
CO1	3	3	3	3	3	3
CO2	3	3	3	3	3	3
CO3	3	3	3	3	3	3
CO4	3	3	3	3	3	3
CO5	3	3	3	3	3	3
3 - Strong; 2 - Medium; 1 - Some						

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Assessment Pattern

(Internal Assessment: 60 Marks + End Semester Examination: 40 Marks)

Internal Assessment (60)					End Semester (40)
Items	**Review 1**	**Review 2**	**Review 3**	**Publication***	
Marks	**5**	**10**	**15**	**30**	**40**
	Total internal marks 60				

K.S.Rangasamy College of Technology – Autonomous R2025								
M.E-VLSI Design								
70 PVL 4P2 - Project Work - Phase II								
Semester	**Hours/Week**			**Total Hrs**	**Credit**	**Maximum Marks**		
	L	T	P		C	CA	ES	Total
IV	0	0	24	360	12	60	40	100

Methodology:

1. The modification proposed in Phase I has to be implemented
2. Three reviews will be conducted by a committee of minimum three members one of which will be the guide
3. Each review has to be evaluated for 100 marks
4. Attendance is compulsory for all reviews. If a student fails to attend the review for some valid reason with proper intimation, one or more chance may be given, else review mark will be zero
5. They should publish the paper preferably in the journals/conferences
6. Final review will be done by the committee that consists of minimum three members one of which should be the guide (including one external expert examiner)
7. The report should be submitted by the students at the end of May

Course Designer(s)

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